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EDN®

Designer's guide to flash-ADC testing—Pt 3

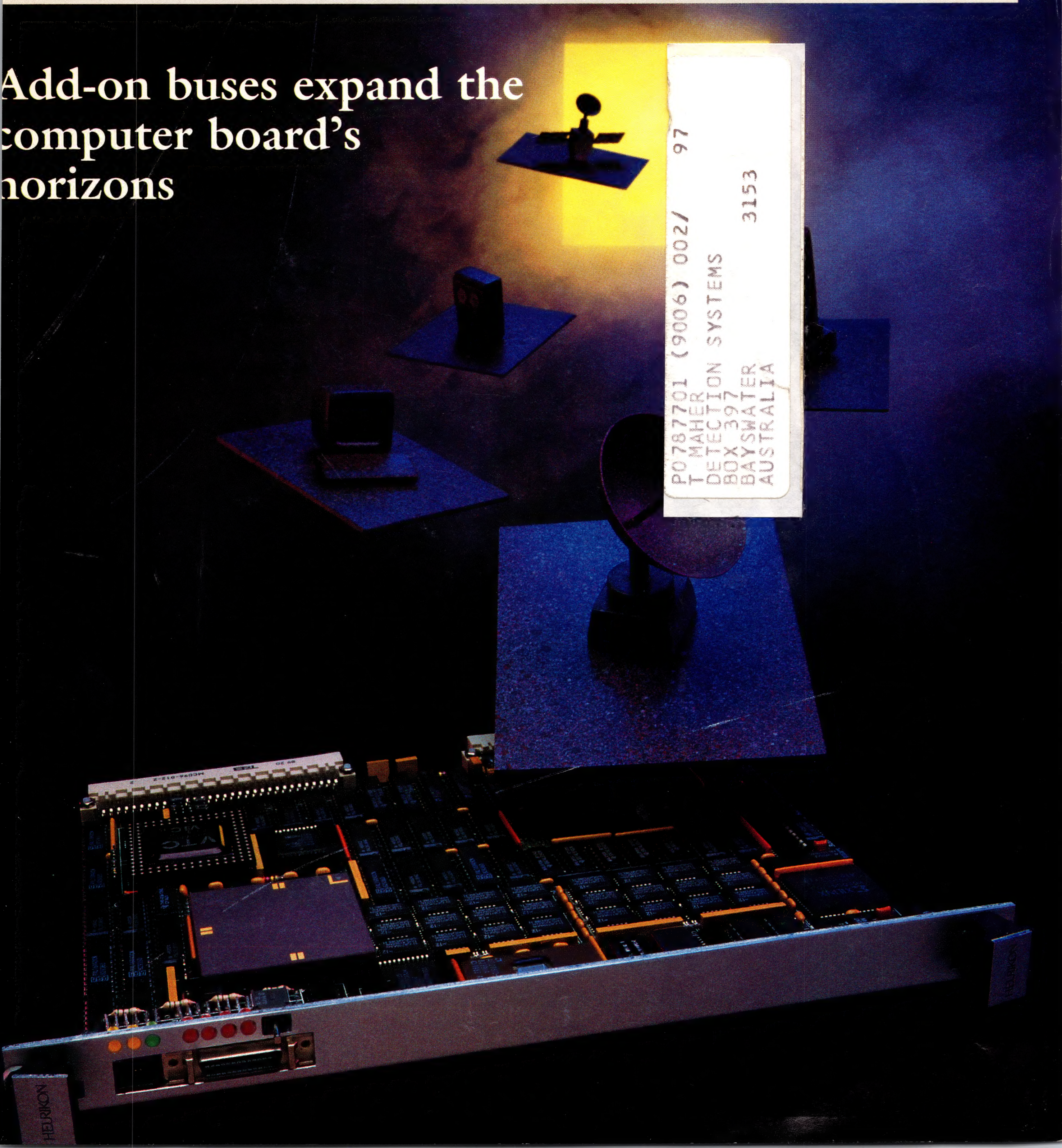
Timing-analysis tools examine delay paths

Designing switch-mode power supplies

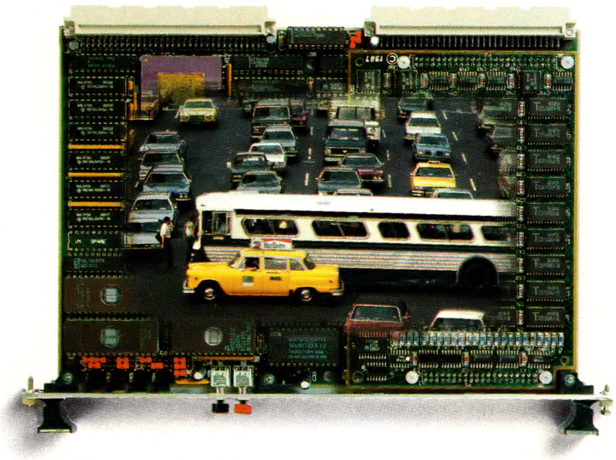
Thermal-analysis software

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

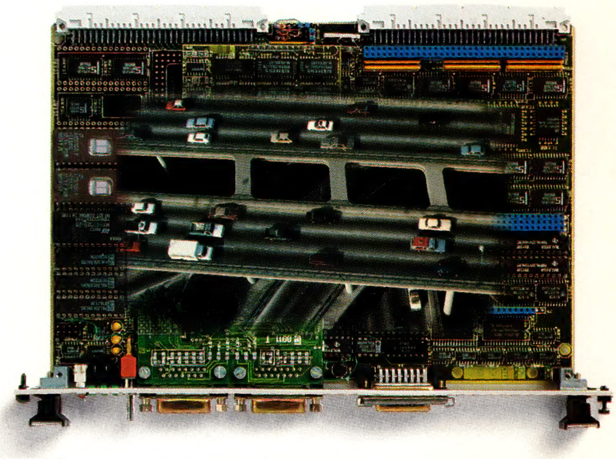
Add-on buses expand the computer board's horizons



THEMIS SINGLE BOARD COMPUTER ELIMINATES DATA-FLOW BOTTLENECKS



Arbitration Delays



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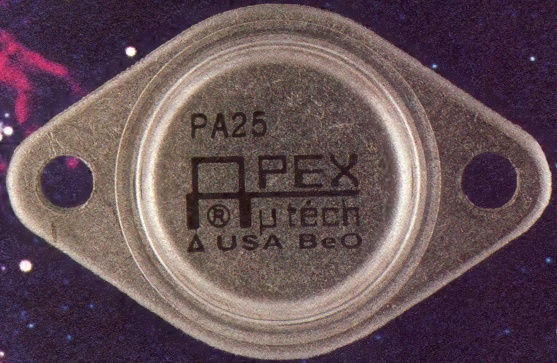

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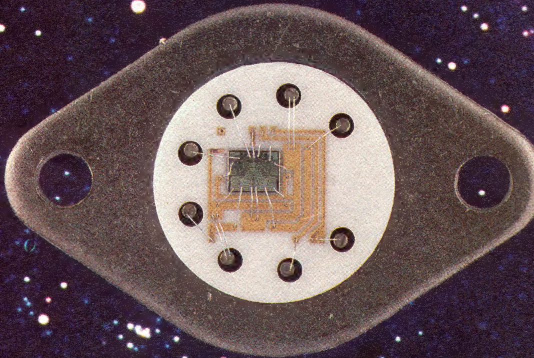

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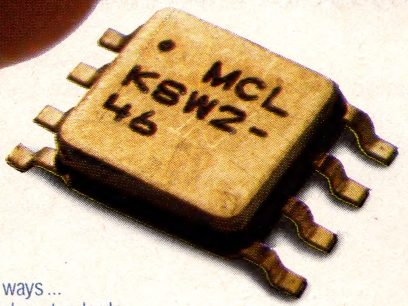
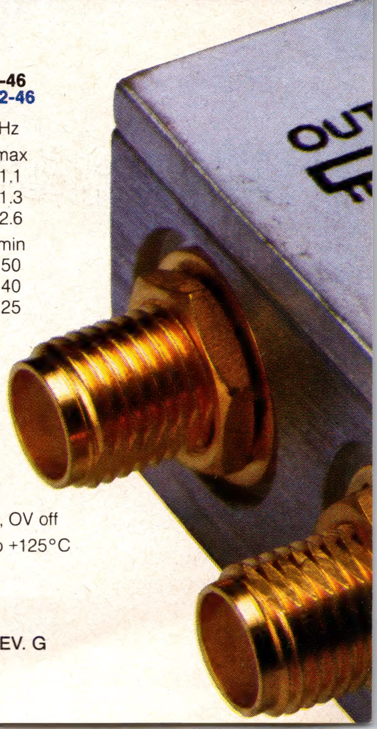


SPECIFICATIONS

Pin Model / Connector Version	**KSW-2-46** / **ZFSW-2-46**		**KSWA-2-46** / **ZFSWA-2-46**	
FREQ. RANGE	dc-4.6 GHz		dc-4.6 GHz	
INSERT. LOSS (db)	typ	max	typ	max
dc-200MHz	0.9	1.1	0.8	1.1
200-1000MHz	1.0	1.3	0.9	1.3
1-4.6GHz	1.3	1.7	1.5	2.6
ISOLATION (dB)	typ	min	typ	min
dc-200MHz	60	50	60	50
200-1000MHz	45	40	50	40
1-4.6GHz	30	23	30	25
VSWR (typ) ON	1.3:1		1.3	
OFF	—		1.4	
SW. SPEED (nsec) rise or fall time	2(typ)		3(typ)	
MAX RF INPUT (bBm)				
up to 500MHz	+17		+17	
above 500MHz	+27		+27	
CONTROL VOLT.	-8V on, OV off		-8V on, OV off	
OPER/STOR TEMP.	-55° to +125°C		-55° to +125°C	
PRICE (10-24)	**$32.95** **$69.95**		**$48.95** **$79.95**	



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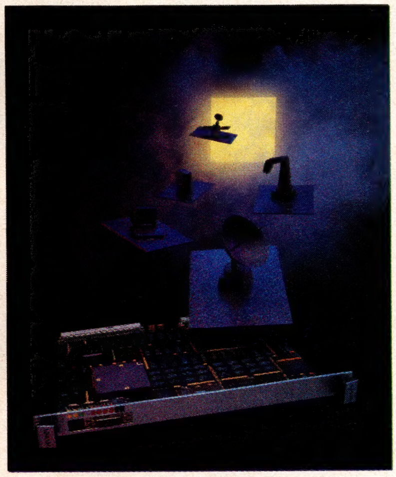
EDN Magazine Edition

Volume 35, Number 3

February 1, 1990

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *Many add-on buses exist to help you expand your computer's capabilities at low cost. However, you should consider the ramifications of choosing a bus that only a few manufacturers support. See the Special Report on pg 82. (Photo concept and production by Heurikon Corp; photography by Ray Perkins Photography)*

SPECIAL REPORT

Add-on buses 82

Add-on buses let you attach small I/O boards to your computer at low cost. However, these devices aren't without controversies, which revolve around technical issues, standards, and just how open the architectures of many add-on buses really are.
—*Jon Titus, Editor*

DESIGN FEATURES

Designer's guide to flash-ADC testing—Part 3 103

The first two parts of this series described the subtleties of flash A/D converters and the test methods used to evaluate these devices. Part 3 concludes the series with a discussion of the actual measurements you'll need to fully characterize flash A/D converters.—*Walt Kester, Analog Devices*

Path-distribution analysis simplifies logic-circuit timing 125

Whereas logic simulators let you prove your circuit does what you want it to, timing-analysis CAD tools provide a more detailed examination of delay paths. Building a design from the results of a simulator without using a timing analyzer is like reading only the beginning of a story—you can't be quite sure how it will turn out.—*Chi-Lai Huang and Marek Ryniejski, Cadence Design Systems Inc*

TECHNOLOGY UPDATES

Switch-mode power-supply ICs: Smart parts let nearly any EE design switchers 29

Although available parts and literature recently made it possible for you to design your own switch-mode power supplies, making a supply that's cost-effective and reliable still requires expertise. You will benefit, however, from learning about this rapidly changing discipline so you can troubleshoot and understand how a supply helps or hinders your system's capabilities.
—*Dan Strassberg, Associate Editor*

Continued on page 7

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CIRCLE NO. 6

Thermal-analysis software: Thermal images provide reliability clues 47

Reliability is critical for products that aren't easily serviced, require extreme safety and precision, and are dangerous to operate. Unfortunately, the delicate relationship between temperature and performance makes predicting reliability tricky. Thanks to new thermal-analysis software for EEs, though, you can identify thermal problems and alter your design before you build it.—*Anne Watson Swager, Associate Editor*

PRODUCT UPDATES

High-performance 32-bit µP 65
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CISC workstations 70

DESIGN IDEAS

Averaging increases µP's ADC resolution 139
Precision amplifier turbocharges buffer 140
Feedback enhances thermometer accuracy 142

EDITORIAL 25

The facsimile machine gives engineers a new way to get information. Soon you can help test an EDN FAX service that will send you product information in seconds.

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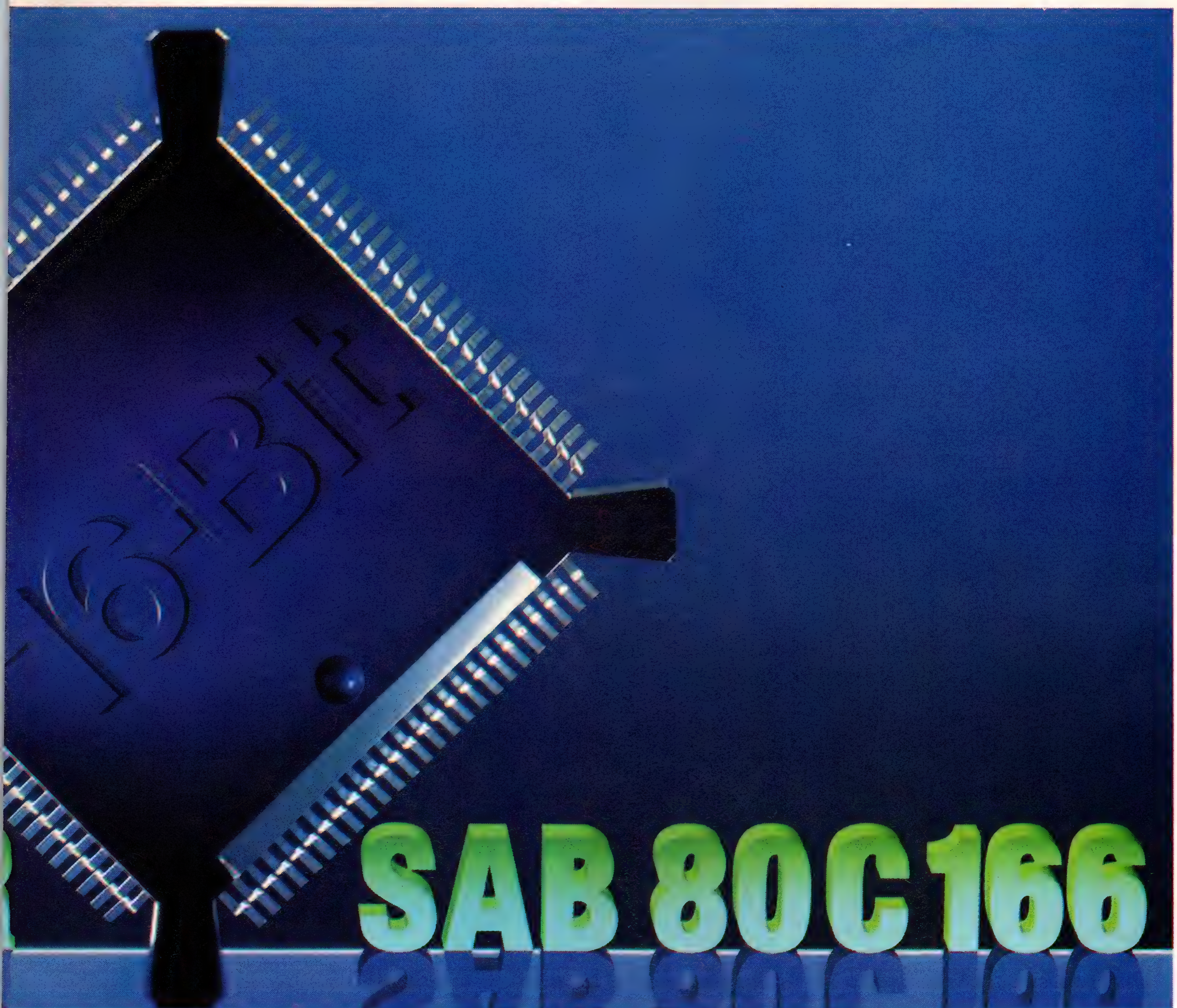

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If that goes down well and you want to find out more, contact your local Siemens office or just write to:

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Even though our products have been to Jupiter and beyond, you can still find them out in your garage.

NEWS BREAKS

EDITED BY JULIE ANNE SCHOFIELD

FIBER-OPTIC DATA LINKS REPLACE CABLES

Concise Technology's (Pontypridd, UK, FAX 603-401158) fiber-optic interfaces can replace RS-232C, RS-422, and RS-423 cards without requiring that you change your communications software. Model CPCFS of the FOSIL (Fiber-Optic Standard Interface Link) 2-cable interface is a short card that fits IBM PC/XT and PC/AT expansion slots; model CVMEFS is a 3U or 6U VMEbus module. The company claims that the interfaces work over a distance of 1.4 miles using 100/140-μm optical fiber at standard baud rates. These cards process all RS-232C signals, control as well as data. The company also offers external repeaters, which let you extend the length of a link. The interfaces cost £175 per channel. The company is developing cards for STE Bus and STD Bus systems. The company hopes that the industry will adopt FOSIL as a standard and will answer any serious inquiries.—Brian Kerridge

VMEbus CPU CARD INCLUDES 50-MHz LOCAL BUS

Heurikon Corp's (Madison, WI, (608) 271-8700) 68040-based Model HK68/V4F VMEbus CPU card includes a 50-MHz 200M-byte/sec synchronous local bus. Called Corebus, this local bus connects the onboard CPU, memory, and I/O subsystems, and provides expansion capability via daughter cards. The card also includes an industry-standard VSB interface with master/slave support. Standard features of the card include 2M to 8M bytes of 70-nsec 2-way-interleaved static-column dynamic RAM and as much as 2M bytes of EPROM. The card also includes 512 bytes of nonvolatile RAM that can store configuration information; the card can address an additional 960M bytes of memory via the VSB interface. I/O capabilities include two RS-232C ports and an optional RS-422 port. You can add support for Ethernet or SCSI via Corebus cards. Software support for the HK68/V4F includes the Unix, OS-9, VRTX, and VxWorks operating systems. A version of the board with a 25-MHz 68040 and 2M bytes of memory will be available the second quarter of this year for $3495. —Maury Wright

PARALLEL COMPUTER OPERATES WITH UNIX SUBSYSTEM

The MP-1 family of data-parallel computers from Maspar Computer Corp (Sunnyvale, CA, (408) 736-3300) consists of eight models. The models have 1024 to 16,384 processing elements (PEs) arranged in a single-instruction, multiple-data (SIMD) array. A distributed-memory architecture provides each PE with its own local memory ranging from 16M to 256M bytes. The computer uses a 500,000-transistor custom ASIC, which includes 32 PEs, the local memory, and the interprocessor interfaces.

The computer communicates with a DEC VAXstation 3520 subsystem, which uses the Ultrix operating system. This combination lets the user create parallel programs using X-Windows for the Unix operating system. The 16,384-PE model delivers as many as 30,000 MIPS and 1250M flops. Prices start at $160,000 for the 1024-PE model; the 16,384-PE model costs $800,000.—John Gallant

NEWS BREAKS

BUY CAE SOFTWARE, GET A WORKSTATION

In a pitch reminiscent of the consumer electronics wars, Racal-Redac (Westford, MA, (508) 692-4900) will give you a Sun Microsystems' (Mountain View, CA, (415) 960-1300) Sparcstation 1 when you purchase its $49,950 Visula Plus CAE software. As an added inducement, the company will also include a 6-month subscription to Logic Automation's (Beaverton, OR, (503) 690-6900) Smartmodels hardware-modeling library. Visula Plus contains a schematic-capture package and the Cadat simulator. It's based on a nonproprietary relational database with structured-query-language (SQL) access.—Michael C Markowitz

RISC μP CHIP SET GETS AN ALTERNATE SOURCE

Since its initial availability in 1986, the Clipper RISC processor has gone through some tough times. National Semiconductor Corp acquired the μP chip set through its purchase of Fairchild Semiconductor Corp and then sold the set to its current owner, Intergraph Corp, forming the core product of Intergraph's Advanced Processor Div (Palo Alto, CA, (415) 852-2365). Now the rough waters seem to be quieting for the μP as a second source, Samsung Electronics Co Ltd (Seoul, Korea, (02) 751-3921), comes on board. Initially, Samsung will fabricate the second-generation C300 chip set and has a worldwide, nonexclusive right to market this product. It expects to begin production in July and will have production volumes in December. The company will also manufacture the first-generation C200 chip set for Intergraph APD and has the option of acquiring marketing rights for this product as well. —Steven H Leibson

VMEbus BACKPLANE TIGHTENS SPECIFICATION

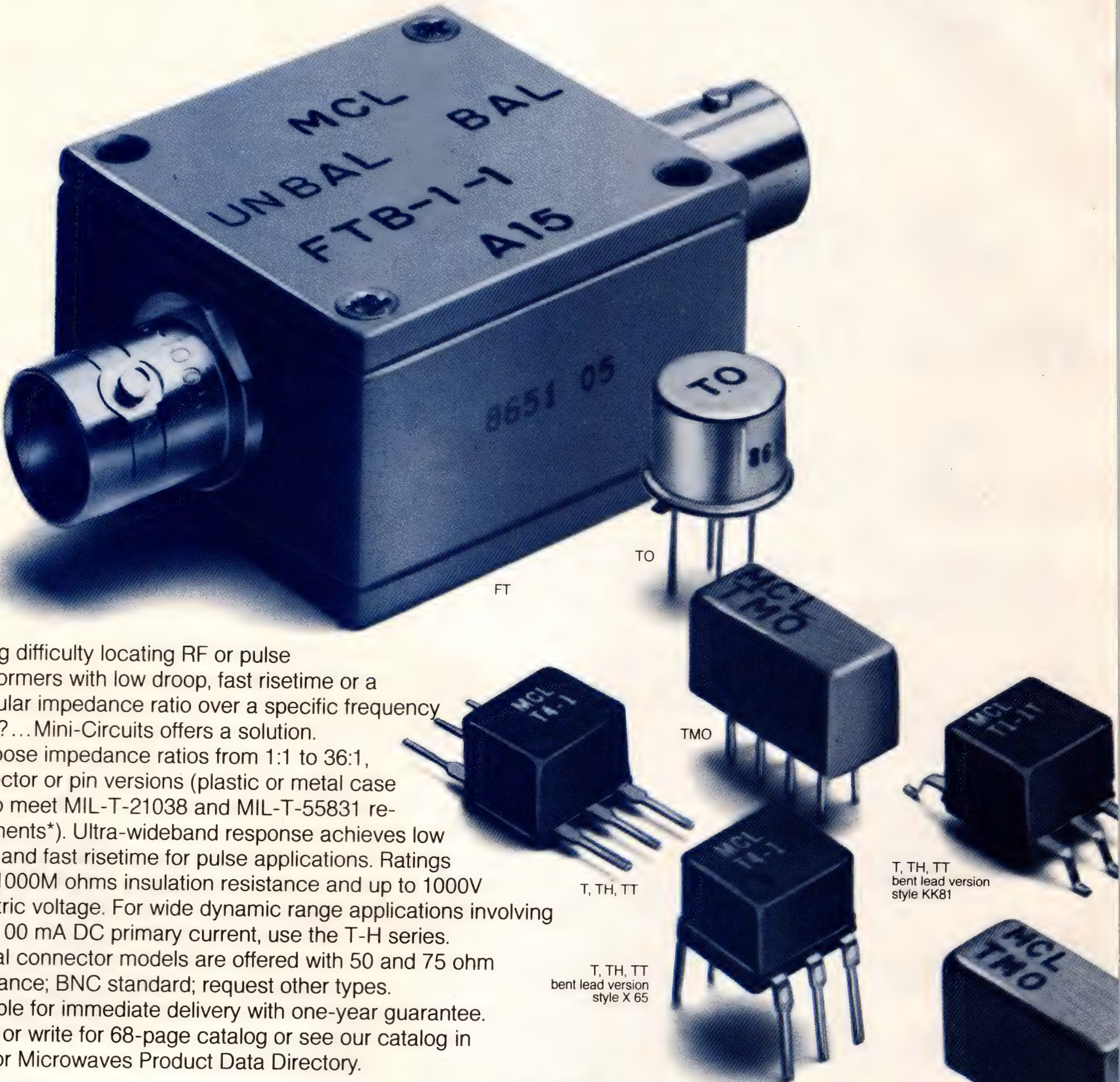
If your VMEbus card cage is running close to its limit, consider the V346/HS VMEbus backplane from Dage (GB) Ltd (Aylesbury, UK, FAX 296-435408). The backplane can withstand harsh environments and lifts card-cage constraints from your VMEbus system's performance. Off-board active-line terminators and a stripline tracking technique guarantee you a characteristic signal-line impedance of $52 \pm 2\Omega$ on all data lines. Insulated 120A busbars are connected to the 0 and 5V rails by studs uniformly distributed across the assembly for uniform, minimized dc resistance. The full-width 21-slot double-height model is available now for £525; 5- and 9-slot versions will follow.—Brian Kerridge

MENTOR TAKES ON A NEW STUDENT AND WORKSTATION

Mentor Graphics (Beaverton, OR, (503) 626-7000) is killing two birds with one stone. Under pressure from Apollo Computer's (since acquired by Hewlett-Packard (Palo Alto, CA, (800) 752-0900)) fall from its perch as the workstation market leader and the consolidation of Cadence Design Systems (San Jose, CA, (408) 943-1234) and Gateway Design Automation, Mentor has responded by announcing the acquisition of Silicon Compiler Systems (San Jose, CA (408) 371-2900) in a deal valued at approximately $110 million. With research facilities in Belgium, England, Japan, Singapore, Oregon, California, Michigan, Utah, and New Jersey, the expanded company will have worldwide development facilities. The move both strengthens Mentor's IC-design and -simulation capability and provides the resources and expertise to port Mentor's tools to Sun Microsystems' (Mountain View, CA, (415) 960-1300) workstations. Mentor Graphics expects to release its products on Sun workstations by late 1990.—Michael C Markowitz

RF TRANS

Over 50 off-the-shelf models...



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T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
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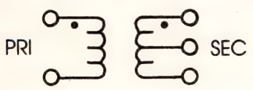
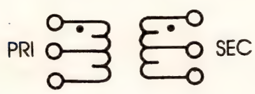
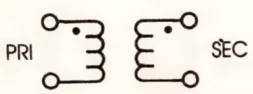
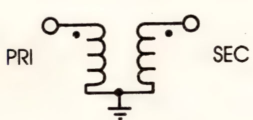
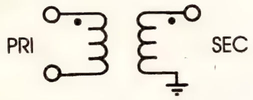
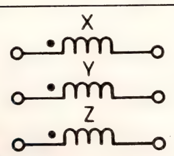
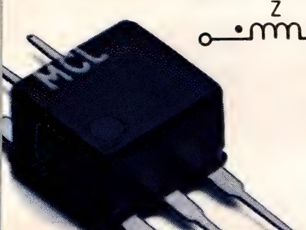
case style number see opposite page		MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS 3dB MHz	2dB MHz	1dB MHz	PRICE $ Qty. (1-9)
A* 	T	T1-1T	1	.05-200	.05-200	.08-150	.2-80	4.45
		T1-6T	1	.003-300	.003-300	.01-150	.02-50	6.95
		T2-1T	2	.07-200	.07-200	.1-100	.5-50	4.95
		T2.5-6T	2.5	.01-100	.01-100	.02-50	.50-20	4.95
		T3-1T	3	.05-250	.05-200	.1-200	.5-70	4.95
		T4-1	4	.2-350	.2-350	.35-300	2-100	3.25
		T4-6T	4	.02-250	.02-250	.05-150	0.1-100	4.45
		T5-1T	5	.3-300	.3-300	.6-200	.5-100	4.95
		T8-1T	8	.03-140	.03-140	.10-90	1-60	7.95
		T13-1T	13	.3-120	.3-120	.7-80	5-20	4.95
		T16-6T	16	.03-75	.03-75	.06-30	.1-20	5.65
	TH	T4-1H	4	10-350	10-350	15-300	25-200	5.95
	TMO	TMO1-1T	1	05-200	.05-200	.08-150	.2-80	7.95
		TMO2-1T	2	.07-200	.07-200	.1-100	.5-50	8.45
		†TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	8.45
		†TMO3-1T	3	.05-250	.05-250	.1-200	.5-70	7.95
		TMO4-1	4	.2-350	.2-350	.35-300	2-100	6.25
		TMO5-1T	5	.3-300	.3-300	.6-200	5-100	8.45
		TMO13-1T	13	.3-120	.3-120	.7-80	5-20	8.45
B* 	TT	TT1-6	1	.004-500	.004-500	.02-200	.1-50	6.95
		TT1.5-1	1.5	.075-500	.075-500	.2-100	1-50	5.95
		TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	6.45
		TT4-1	3	.05-200	.2-50	.2-50	1-30	5.95
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95
		TT25-1	25	.02-30	.02-30	.05-20	.1-10	9.95
	TTMO	TTMO25-1	25	.02-30	.02-30	.05-20	.1-10	11.95
		TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	11.45
		TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95
C 	T	T1-1	1	.15-400	.15-400	.35-200	2-50	3.25
		T1.18-3	1.18	0.01-250	0.01-250	0.02-200	0.03-50	5.65
		T1-6	1	.01-150	.01-150	.02-100	.05-50	5.65
		T1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	4.45
		T1.5-6	1.5	.02-100	.02-100	.05-50	0.1-25	5.65
		T2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	4.45
		T4-6	4	.02-200	.02-200	.05-150	.1-100	4.45
		T9-1	9	.15-200	.15-200	.3-150	2-40	3.95
		T16-1	16	.3-120	.3-120	.7-80	5-20	4.45
		T36-1	36	.03-20	.03-20	.05-10	.1-5	6.95
	TO	TO-75	1	10-500	—	10-500	40-250	6.95
	TH	T1-1H	1	8-300	8-300	10-200	25-100	5.95
		T9-1H	9	2-90	2-90	3-75	6-50	6.45
		T16-H	16	7-85	7-85	10-65	15-40	6.45
	TMO	TMO1-02	1	1-800	1-800	2-500	—	9.45
		TMO1-1	1	.15-400	.15-400	.35-200	2-50	6.25
		TMO1.5-1	1.5	.1-300	.1-300	.2-150	.5-8	8.45
		†TMO2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	7.95
		†TMO4-6	4	.02-200	.02-200	.05-150	.1-100	7.95
		TMO6-1	6	.3-200	.3-200	.5-150	5-50	7.95
		TMO9-1	9	.15-200	.15-200	.3-150	2-40	7.95
		TMO16-1	16	.3-120	.3-120	.7-80	5-20	7.95
D 	T	T2-1	2	.050-600	.050-600	.1-400	.5-200	3.95
		T3-1	3	.5-800	.5-800	2-400	—	4.45
		T4-2	4	.2-600	.2-600	.5-500	2-250	3.95
		T8-1	8	.15-250	.15-250	.25-200	2-100	3.95
		T14-1	14	.2-150	.2-150	.5-100	2-50	4.95
	TMO	TMO2-1	2	.050-600	.050-600	.1-400	.5-200	7.95
		TMO3-1	3	.5-800	.5-800	2-400	—	8.45
		TMO4-2	4	.2-600	.2-600	.5-500	2-250	7.95
		TMO8-1	8	.15-250	.15-250	.25-200	2-100	7.95
		TMO14-1	14	.2-150	.2-150	.5-100	2-50	8.45
	FT	FT1.22-1	1.22	.005-100	.005-100	.01-50	.05-25	35.95
		FT1.5-1	1.5	.1-400	.1-400	5-200	1-100	35.95
E 	FTB	FTB-1	1	.2-500	.2-500	.5-300	1-100	36.95
		FTB1-6	1	.01-125	.01-125	.05-50	.1-25	36.95
		■FTB-1-75	1	.5-500	.5-500	5-300	10-100	36.95
F 	T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25
		T626	1	0.01-10	0.01-10	0.2-5	.04-2	3.95

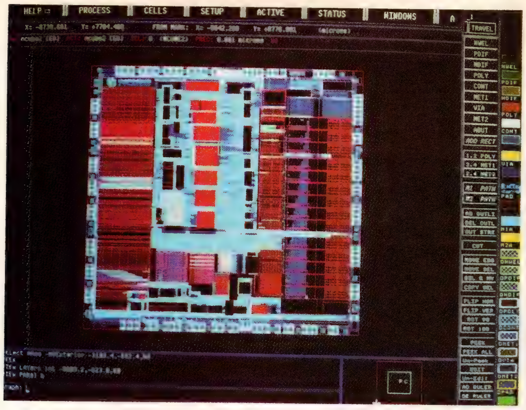


■ Denotes 75 ohm models

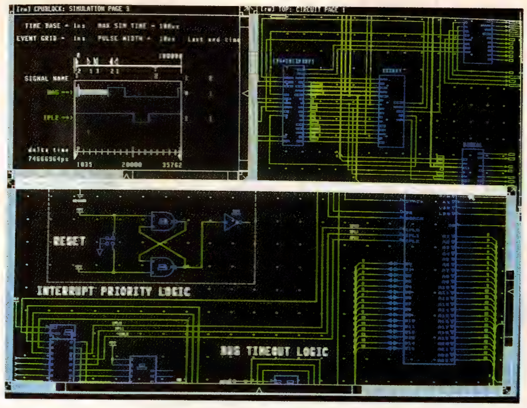
* FOR A AND B CONFIGURATIONS

Maximum Amplitude Unbalance
- 0.1 dB over 1 dB frequency range
- 0.5 dB over entire frequency range

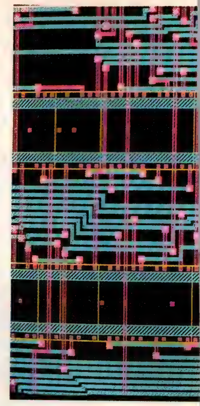
Maximum Phase Unbalance
- 1.0° over 1 dB frequency range
- 5.0° over entire frequency range



Mentor Graphics delivers a broad line of integrated EDA software, including advanced custom and semicustom IC tools.



HP DesignCenter provides integrated tools for digital, analog, and microwave circuits, as well as ME CAD and CASE.



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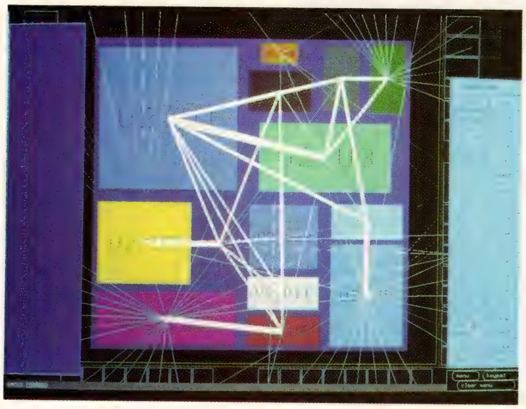
high-performance
integrated desig



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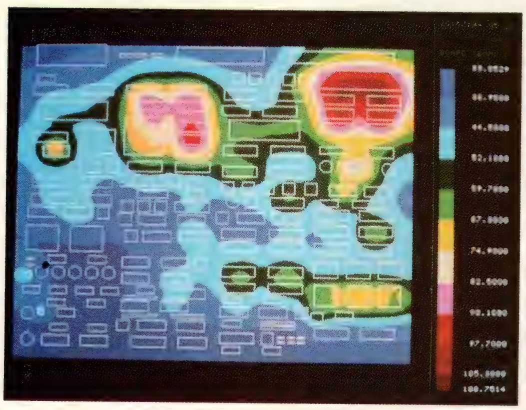
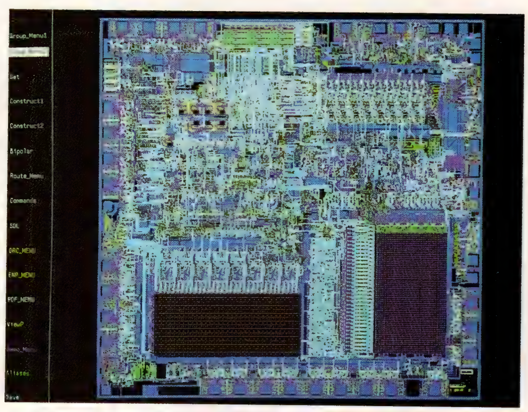
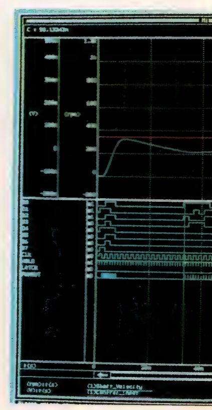


Pacific Numerix concurrent engineering solutions simulate the performance and manufacturability of PCB designs.



Silicon Compiler Systems' ASIC and IC design tools support all phases of design in an open framework.



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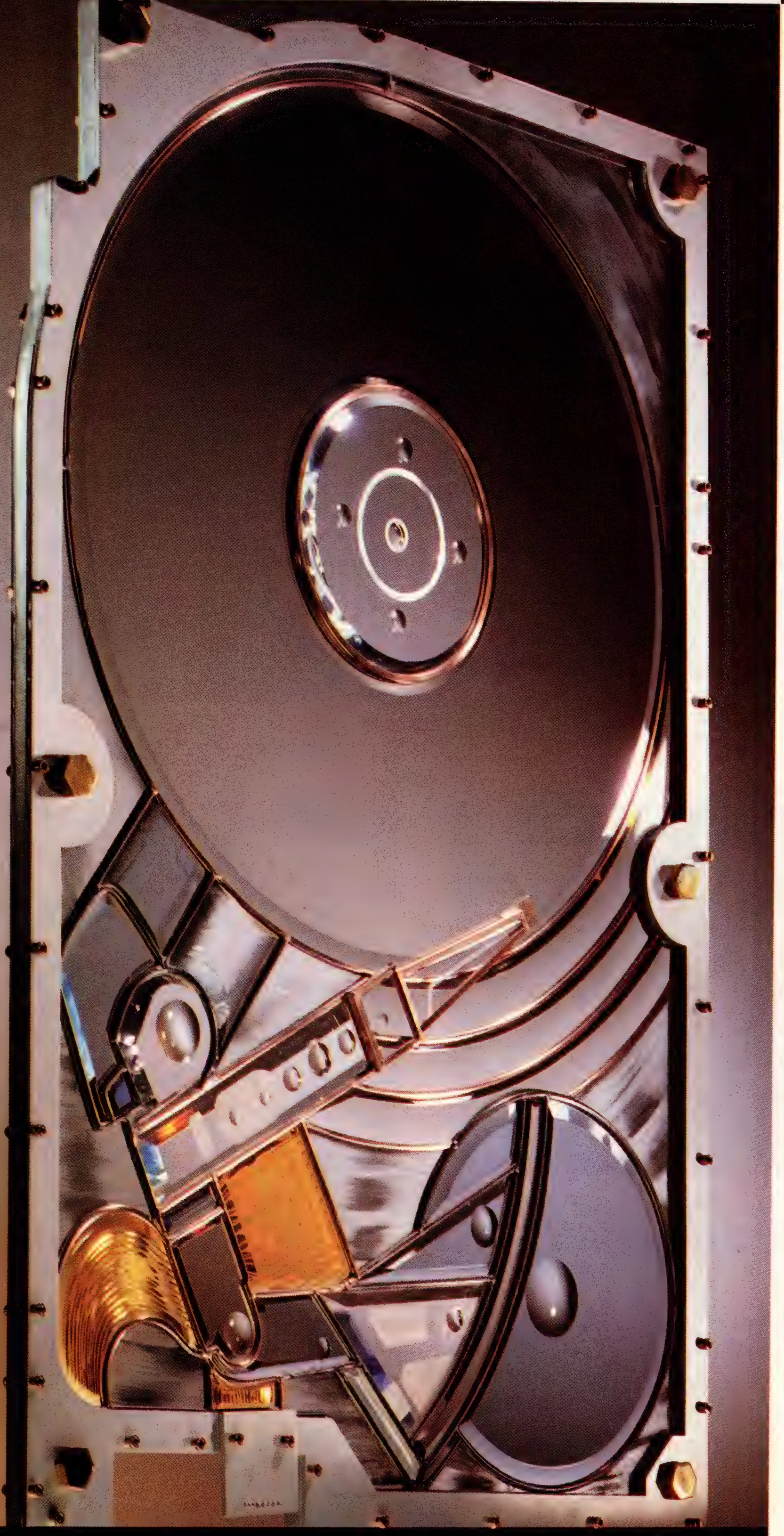

Beveled Glass Window by
Thomas Tisch & Andreas Lehmann
Oakland, California

Even to the experienced observer, a disc drive is a technological marvel. With discs spinning at 60 revolutions per second, the mechanics involved are astounding. It takes a company with a unique level of skill and experience to produce drives in volume that perform reliably year after year. A company like Seagate.

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Although FAX machines have been available for years, only during the last year have they become widespread in business and industry. Many mail-order firms now let you place orders by FAX, and you can send binding signed documents by FAX. The popularity of FAX communications is apparent in advertisements and product announcements, too. A year ago, few advertisers put FAX numbers in their ads. Today, there are few ads that don't furnish a FAX number. FAX numbers also show up in new-product announcements, on business cards, and on letterhead.

FAX transmissions are changing the way engineers communicate, too. We can transmit schematics, sketches of prototypes, and product information by FAX. Also, several companies already offer a fast-inquiry service that transmits product literature to you via FAX. And, several magazines offer reader-service cards that you can return via FAX. However, those services don't fulfill the promise of a FAX unit. You should be able to get information quickly on many products from a single data service.

In our next issue, you'll find a special reader-service card that you can return by FAX. That card does more than bypass the postal service's link between us. When you return the "card" by FAX, our computer scans it, selects stored FAX images of the literature you need, and returns it to your FAX within a minute or two. Thus, if you need information about an advertised computer board and a switching power supply, you can get both—from different suppliers—within minutes. Keep in mind that this is a test, so we've limited the first FAX-inquiry card to a handful of advertisers. If you like and use the service, we'll expand the system.

Obviously our FAX system isn't going to dump a complete 300-pg CMOS databook to your machine. But you will get four to five pages of pertinent information about advertisers' products. I remember waiting six to seven weeks to get information via a reader-service postcard. Even when I called a sales office it could take weeks to get spec sheets. Using a central FAX service puts you in immediate contact with companies and their products.

As part of the FAX test, I want to know more about your access to and use of FAX machines. Please read the statements below and circle the corresponding numbers on one of our reader-service cards. Sorry, no FAX responses; instead, I'll let our card-processing people tabulate the results.

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FAX machine is within a 1-minute walk of my office.	**Circle No. 693**
I send/receive information via FAX.	**Circle No. 694**

Thanks for your help.

Jon Titus
Editor

Jesse H Neal
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1987, 1981 (2), 1978 (2),
1977, 1976, 1975
American Society of
Business Press Editors Award
1988, 1983, 1981


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CIRCLE NO. 27

SWITCH-MODE POWER-SUPPLY ICs

Smart parts let nearly any EE design switchers

Though you can design switchers yourself, you'll probably want to call on experts for cost-effective, reliable supplies that emit low EMI and meet international safety standards.

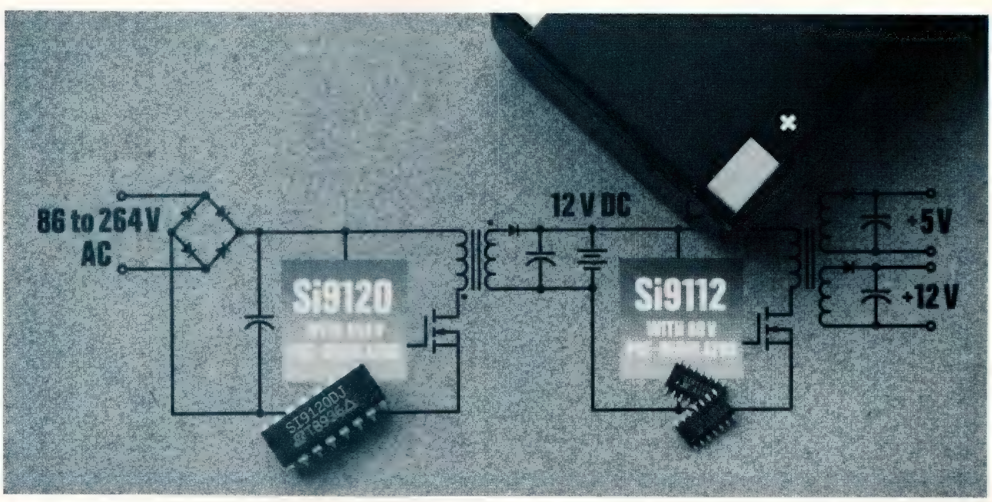
Dan Strassberg,
Associate Editor

Designing switch-mode power supplies isn't what it used to be. Once the private preserve of only a few thousand specialists throughout the world, it has turned into an arena in which any number can play. Thanks to the increasingly intelligent ICs and a torrent of applications literature spewing forth from a score of vendors, nearly any electronic engineer with hardware-design experience can create an ac-line-to-dc switcher or a dc-dc converter that works. But, except for the lowest performance applications, making a supply that not only works, but also is cost-effective and reliable, reproducible in volume, and meets worldwide EMI and safety standards usually still requires specialized expertise.

Furthermore, if, for example, your job is designing μP-based systems, your employer has every right to ask whether power-supply design represents an appropriate use of your time. What's more, building power supplies isn't necessarily an effective use of your company's manufacturing resources; purchasing the supplies you put in your products might make a lot more sense. (A possible exception—a type of supply you should consider designing and building—is a nonisolated, low-power, dc-dc converter mounted on a primarily digital pc board to power functions that require supply voltages different from those available in your system.)

Learn, don't burn

Even if you decide to relegate most or all of your power-supply design activities to "government jobs," learning more about modern power-supply architecture can be worth your effort: when

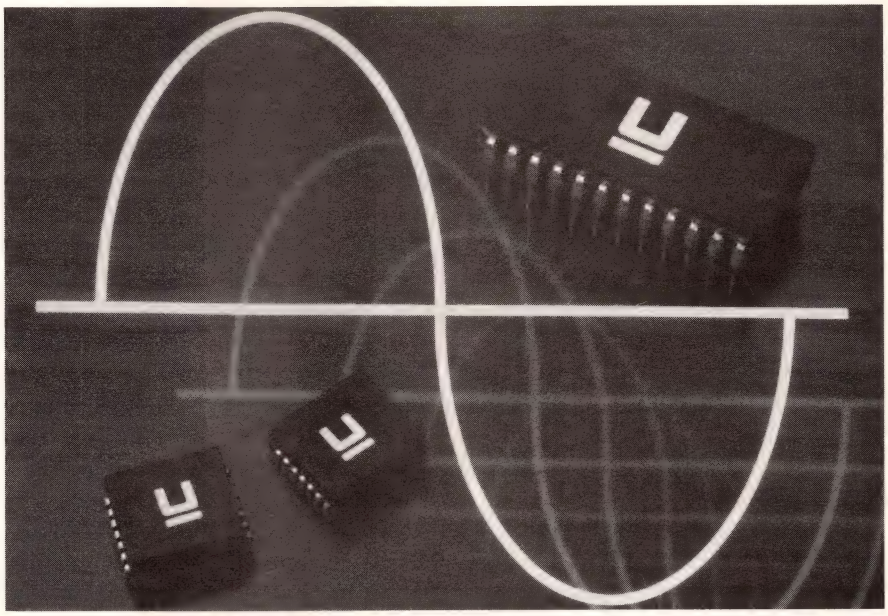


***A 450V preregulator** in Siliconix's Si9120 allows you to create "universal-input" switch-mode supplies that operate from 50-to-450V rectified ac lines without having to reconnect the rectifiers. With an 80V preregulator, the Si9112 is for battery-powered equipment that operates from 9 to 80V dc.*

Switch-mode power-supply ICs

systems misbehave, understanding how a power supply might lie at the root of the problem can save precious troubleshooting time. (For example, a switcher can inject ripple current into the ground reference of a noise-sensitive circuit.) Moreover, in this era of digital techniques, many EEs tend to ignore the physics of the circuits they work on, and few areas of electronics bring home the importance of the physical limitations of circuit layouts and devices as clearly as does switching power-supply design.

If you set out to become a self-taught switching-power-supply expert, you will quickly realize that you've tackled a problem of continuing self education. In switching power supplies, as in most areas of electronics, the only constant is change. Techniques that were mainstays just three years ago appear much less often in today's designs.



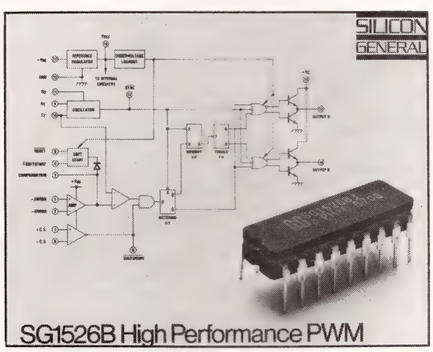
***Surface-mount technology** is appearing in more and more switch-mode supplies. Unitrode's UC3860 resonant-mode control chip answers supply designers' demands for packaging flexibility. The vendor provides it in a 28-pin PLCC and a 24-pin DIP.*

Switch to the fast track

When most supplies used linear technology, the power-supply field was slow to change. Today, the pace of change is rapid—perhaps too rapid. New design approaches sometimes exhibit new failure modes; the industry can take several years to recognize and correct those modes. Such a situation occurred a decade ago when the first power MOS switches appeared. Unless your requirements are very unusual, because reliability is so important in power supplies, you can frequently justify a wait-and-see attitude toward adopting new approaches.

An area where many observers feel that a go-slow posture will prevail is acceptance of resonant-mode conversion. In supplies that use most of the older pulse-width-modulated (PWM) architectures, the switching frequency remains relatively constant; the percentage of time that the switching elements conduct varies in response to changes in the input voltage and the load current. In resonant supplies, the switches conduct for a constant period of time—determined by the half period of a tank circuit's resonant frequency. These supplies achieve regulation by varying the frequency at which the switches operate (**Refs 1** and **2**).

If a power-supply design's success depended only on semiconductors, designers would be quicker to adopt the resonant-mode conversion ICs that have reached the market within the past few years. But there are many elements besides semiconductors in most successful power-supply designs: Magnetic components must have the necessary inductance and distributed capacitance under all operating conditions. Capacitors must be correctly applied (for example, to prevent ripple current from causing them to overheat). Temperature rises must be properly managed and conducted. Radiated interference must be adequately limited. Printed circuits must be laid out and magnetic components must be designed to meet spacing requirements imposed by the agencies that set safety standards.



***With a complementary output,** soft-start and undervoltage-lockout circuits, a sync pin, and an internal reference, Silicon General's SG1526B incorporates most of a PWM supply's functional blocks.*

Over the years that PWM has dominated the switching-power-supply field, despite the relentless upward trend in switching frequencies, EEs throughout the industry have become familiar with how to select a supply's entire component complement. In resonant supplies, the role of many of the components,

particularly inductors and capacitors, is especially critical. Notwithstanding a growing body of applications literature, designers and component vendors need time to become as familiar with resonant-supply components as they are with PWM-supply components. Therefore, if you're designing your first switch-mode power supply, bear in mind that you stand a better chance of getting the information you need to develop a reliable supply if you choose PWM conversion.

Know-how yields reliability

If, however, you're convinced that your system should use a resonant-mode power supply (for example, to obtain a power density greater than 20W/in.^{3} from a single supply that produces an output below ~ 200W), you can obtain a supply with the requisite reliability by purchasing it from a vendor with several years' experience building such units. A few power-supply vendors already know a great deal about how to design reliable resonant-mode supplies.

Although its technology is a revolutionary departure from traditional design approaches, in several respects resonant-mode conversion represents a continuation of trends that have dominated the switching-power-supply field since its inception. These trends, toward increased power density and increased switching frequency, affect PWM as well as resonant-mode supplies. Lately, in addition, the power-supply industry has had to meet user demands for greatly improved reliability.

By permitting size reductions in magnetic components and capacitors, increased switching frequency has made possible increased power density. However, if you hold a supply's output and efficiency constant while reducing its size, the operating temperature of the components will increase and the supply's reliability will decrease—unless you can devise new techniques for thermal management.

Opinions vary on whether further increases in the switching-frequency capabilities of PWM-supply ICs really will make possible additional meaningful reductions in the size of magnetic components and of the supplies themselves. At least in the short run, several factors militate against actually operating supplies at higher frequencies and thus, against realizing the ICs' promise of reductions in supply size:

- Keeping magnetic-core losses low with faster switching requires improved magnetic materials optimized for higher frequency operation.
- In line-operated supplies, the rules of regulatory agencies, such as Underwriters' Laboratories, govern the spacing between the primary and secondary windings of transformers that provide isolation.
- Simultaneously achieving higher speed and lower on-resistance in power MOSFET switches requires improvements in semiconductor processing technology.

Furthermore, removing heat from high-power-density supplies requires innovative thermal design. In designs that rely on natural con-

Table 1—Partial list of switch-mode power-supply IC vendors[1]

Vendor	Circuit types: Voltage mode	Current mode	Resonant mode	Low standby power	Power-factor correction	Notes
Cherry	•	•	•			
Gennum		•	•			
Harris	•					2
Hitachi America	•	•				3
Lambda	•					4
Linear Technology	•					
Maxim				•		
Micro Linear	•	•			•	5
Motorola	•	•	•			3
National	•					3, 4
Raytheon				•		
SGS-Thomson	•	•				3
Siemens				•		
Silicon General	•	•				3, 6
Siliconix	•			•		7
Teledyne		•		•		
Unitrode	•	•	•		•	3

Notes:
1. This table lists only those circuit types that vendors initially introduced after EDN last surveyed the entire switch-mode IC field in July 1987. Consult vendors for circuit types introduced earlier.
2. Harris supplies a 2-chip set for isolated ac-to-dc supplies and a 1-chip device for building a complete nonisolated ac-line-operated dc supply.
3. This vendor also supplies high-frequency PWM controllers that operate at or above 200 kHz.
4. In addition to monolithic parts, vendor supplies hybrid devices that include both PWM control and medium power switches.
5. Micro Linear's PWM controllers are high-speed devices. The firm also supplies a configurable power-controller array.
6. Silicon General also supplies low-voltage supervisory circuits and switching-regulator power-output stages.
7. Siliconix supplies devices that operate without step-down transformers from rectified ac lines with dc values as high as 450V.

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☐ **Highest density:** CGA 70E18: 12,800 equivalent gates
CGA 40E12: 7,752 equivalent gates
CGA 1ME12: 4,584 equivalent gates and 1280 bits of RAM.

☐ **Performance:** Superior speed/power performance—<0.1 pJ; 300 ps delay; 300 μW power dissipation (typical gate).

☐ **Ease of design:** Raytheon's contiguous row array topology provides a superior design approach when compared to fixed position cell-based technologies. This topology offers greater flexibility and ease in macrocell design, placement and routing.

☐ **Interface capability:** I/Os compatible with ECL (10 KH or 100 K), TTL, CMOS, ETL (mixed ECL and TTL), and ETC (mixed ECL, TTL and CMOS).

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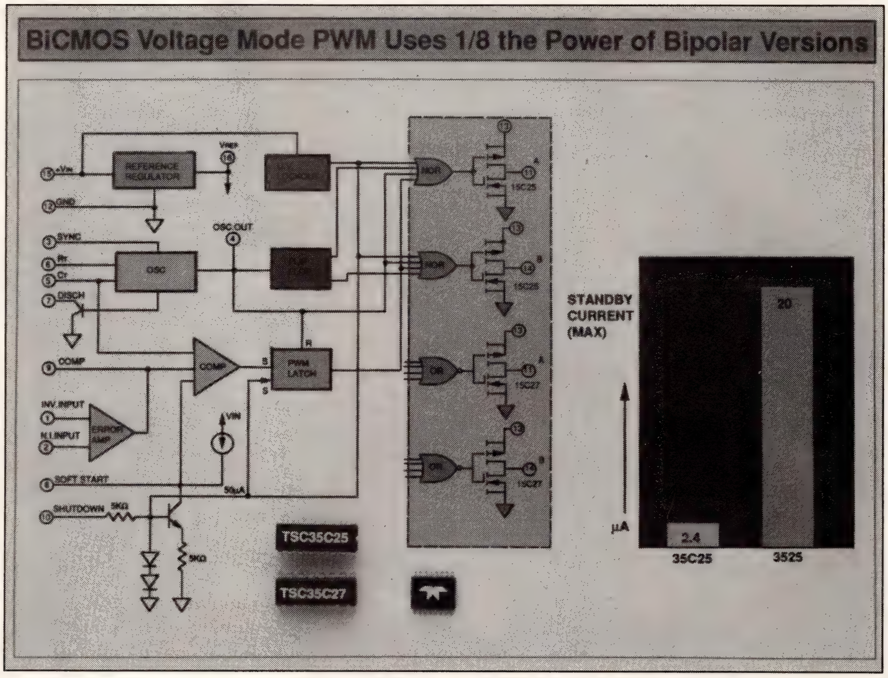
vection in air, increased power density is often merely an illusion. Supplies that quote spectacularly high power densities often do so by passing on to you the responsibility for maintaining an acceptably low case temperature. If you want to realize a significant fraction of such supplies' rated output, unless you can use an unconventional cooling technique, such as forced-air, liquid, or vapor-phase cooling, you must attach large, heavy heat sinks to the supplies, Once you have done so, the power density you achieve from the combination of heat sinks and power supplies is usually not spectacular at all.



Using a BiCMOS process *enables Teledyne Semiconductor to cut the standby power consumption of its TSC35C25 and TSC25C27 pulse-width modulators to ⅛ that of the bipolar versions.*

Factor in the power factor

An area related to efficiency is power factor. A popular misconception has it that the reason most ac-line-operated switching supplies exhibit power factors much below unity is that their input current is out of phase with the line voltage. In fact, the reason is that their input current is highly nonsinusoidal. Because the supplies directly connect the rectified ac line to filter capacitors that store a great deal of energy, the rectifiers only conduct for a short interval every half cycle near the instantaneous line-voltage peak. The resulting input-current waveform is a series of pulses at twice the line frequency. The integral of the product of the instantaneous input current and voltage over one line-voltage cycle represents the energy delivered to the supply during the cycle. That value divided by the cycle's duration is the input power.

The input power is much less than the product of the rms line voltage and the rms input current. To obtain the power factor (PF), you divide the input power by the rms-line-voltage/rms-input-current product. PF values of 0.6 are not uncommon in high-power switching supplies. If a supply operating from an ac line whose nominal rms value is 115V and whose minimum value is 100V produces a dc output of 1000W with an efficiency of 80% and a power factor of 0.6, the supply will draw 20A at low line voltage under a full load. A similar supply with PF of 1 draws only 12A under the same conditions. The standard 3-wire, grounded ac receptacles used in the US are rated for only 15A. Thus, a piece of equipment using the unity PF supply can operate from a building's existing wiring. With the 0.6 PF supply, the unit requires special ac wiring.

ICs correct power factor

It's clear that there are many instances where a supply's power factor can be important. Until recently, power-factor correction required bulky, expensive, passive components. Now, however, IC vendors have begun introducing power-factor correction ICs. The cost of these devices is justifiable in many more situations than is the cost of passive power-factor correction networks. The ICs exact a minimal penalty on efficiency and they're much smaller than the passive components you'd have to use to do the same job.

In addition to the trends already discussed, the switch-mode power-supply IC market is seeing trends toward more complete integration of supply functions onto single chips and toward control chips that consume less power. The **box**, "For more information . . . ," lists many of the vendors of switch-mode power supply ICs; **Table 1** indicates types of ICs these vendors have introduced since EDN last surveyed the field—July of 1987. The **table** provides an indication of where vendors have placed their power-supply IC development effort for the past 2½ years. The trends toward more complete integration and lower-power control chips reflect a quest for improved reliability.

Supposedly objective data indi-

WESTCOR STAKPAKS™. WORLD'S SMALLEST SINGLE OR MULTIPLE OUTPUT, FAN-COOLED SWITCHERS. THE STAKPAK: 1200 WATTS— 3.2" x 5.5" x 11.5" CASE. STAKPAK II: 600 WATTS— 1.9" x 5.5" x 12" CASE.

Westcor's compact and low profile StakPaks redefine power packaging with unprecedented power density and output flexibility. Patented megahertz module technology provides up to 6 watts/cubic inch and up to 8 isolated and fully regulated outputs (5 outputs for StakPak II) while at the same time guaranteeing high reliability and reduced time to market.

Consider these standard features:

- Standard or custom outputs (2-95 VDC)
- UL, CSA, VDE (TUV) Safety Agency Approved (StakPak II in process)
- 80% Efficient, typical
- 110/220 VAC, fool-proof strapping
- Full power @ 40°C

Please contact Westcor for datasheets, pricing and additional information.

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Los Gatos, CA 95032
(408) 395-7050 • FAX (408) 395-1518

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STAKPAK II STANDARD 600 WATT MODELS

Model	Output Voltage (VDC) and Maximum Current (amperes) per Channel				
	#1	#2	#3	#4	#5
Single Output					
ST1-1401	2 @ 120				
ST1-1402	5 @ 120				
ST1-1301	12 @ 50				
ST1-1302	15 @ 40				
ST1-1303	24 @ 25				
ST1-1304	28 @ 21				
ST1-1305	48 @ 13				
Dual Output					
ST2-1401	2 @ 60	5 @ 60			
ST2-1402	5 @ 60	5 @ 60			
ST2-1403	5 @ 60	12 @ 33			
ST2-1404	12 @ 33	12 @ 33			
ST2-1405	15 @ 26	15 @ 26			
Triple Output					
ST3-1401	5 @ 60	12 @ 16	12 @ 16		
ST3-1402	5 @ 60	15 @ 13	15 @ 13		
ST3-1501	5 @ 90	12 @ 8	12 @ 8		
Quad Output					
ST4-1401	5 @ 30	12 @ 16	12 @ 16	5 @ 30	
ST4-1402	5 @ 30	15 @ 13	15 @ 13	5 @ 30	
ST4-1403	5 @ 30	12 @ 16	12 @ 16	24 @ 8	
ST4-1501	5 @ 30	15 @ 13	15 @ 13	24 @ 8	
ST4-1502	5 @ 60	12 @ 16	12 @ 8	5 @ 15	
ST4-1503	5 @ 60	15 @ 13	15 @ 7	5 @ 15	
ST4-1504	5 @ 60	12 @ 16	12 @ 8	24 @ 4	
ST4-1505	5 @ 60	15 @ 13	15 @ 7	24 @ 4	
Five Output					
ST5-1501	5 @ 30	12 @ 16	12 @ 16	5 @ 15	24 @ 4
ST5-1502	5 @ 30	15 @ 13	15 @ 13	5 @ 15	24 @ 4

Total output power may not exceed 600 watts for any model, single or multiple output. Lower power StakPak II models and many other configurations are available. Please contact the factory.

CIRCLE NO. 28

STAKPAK STANDARD 1200 WATT MODELS

Model	Output Voltage (VDC) and Maximum Current (amperes) per Channel				
	#1	#2	#3	#4	#5
Single Output					
SP1-1801	2 @ 240				
SP1-1802	5 @ 240				
SP1-1803	12 @ 100				
SP1-1604	15 @ 80				
SP1-1605	24 @ 50				
SP1-1606	28 @ 42				
SP1-1607	48 @ 25				
Dual Output					
SP2-1801	2 @ 120	5 @ 120			
SP2-1802	5 @ 120	5 @ 120			
SP2-1803	5 @ 120	12 @ 66			
SP2-1804	12 @ 66	12 @ 66			
SP2-1805	15 @ 53	15 @ 53			
Triple Output					
SP3-1801	5 @ 180	12 @ 16	12 @ 16		
SP3-1802	5 @ 150	12 @ 33	12 @ 16		
SP3-1803	5 @ 180	15 @ 13	15 @ 13		
SP3-1804	5 @ 150	15 @ 26	15 @ 13		
Quad Output					
SP4-1801	5 @ 150	12 @ 16	12 @ 16	5 @ 30	
SP4-1802	5 @ 150	15 @ 13	15 @ 13	5 @ 30	
SP4-1803	5 @ 150	12 @ 16	12 @ 16	24 @ 8	
SP4-1804	5 @ 150	15 @ 13	15 @ 13	24 @ 8	
Five Output					
SP5-1801	5 @ 120	12 @ 16	12 @ 16	5 @ 30	24 @ 8
SP5-1802	5 @ 120	15 @ 13	15 @ 13	5 @ 30	24 @ 8
Seven Output					
SP7-1801	5 @ 60	12 @ 16	12 @ 16	24 @ 8	24 @ 8
	#6	#7			
	5.2 @ 28	2 @ 30			

Total output power may not exceed 1200 watts for any model, single or multiple output. Lower power StakPak models and many other configurations are available. Please contact the factory.

cates that in real applications, switch-mode power supplies are less reliable than linear supplies. Much of the data has problems, though. Few of the comparisons relate the MTBF of units providing equal outputs under equivalent conditions. Linear-supply efficiency averages around 45%; for switchers, efficiency usually exceeds 70%. So, if you have a linear supply and a switcher each producing a 100W output, the linear supply will dissipate 120W. The switcher will dissipate only about 40W and will therefore exhibit a lower temperature rise. The switcher's cooler operation will tend to improve its reliability. And, though not related to reliability, the switcher's size and weight will be much lower than those of the linear supply.

Nevertheless, a unit's failure rate does correlate with the number of components it uses, and most switching supplies use many more components than do linear supplies that produce equivalent output power. Placing more of the supply circuits on a single IC chip ought to improve reliability.

Reducing the power dissipated in a switch-mode power-supply control chip will also improve a supply's reliability, although usually not dramatically. In most supplies, the control chip and the voltage-dropping resistors in series with the chip's power-input pin do not dissipate a significant part of the power the supply consumes. In regulators for battery-powered equipment, though, the situation can be quite different. Moreover, although reliability is often a paramount consideration in such equipment, extending battery life is usually even more important. New control ICs, includ-

For more information . . .

For more information on the switching-regulator ICs discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service. When you contact any of the following vendors directly, please let them know that you read about their products in EDN.

Cherry Semiconductor
2000 South County Trail
East Greenwich, RI 02818
(401) 885-3600
FAX 401-885-5786
Circle No. 715

Gennum Corp
Box 489, Station A
Burlington, Ontario, Canada L7R 3Y3
(416) 632-2996
FAX 416-632-2055
Circle No. 716

Harris Semiconductor
Box 883
Melbourne, FL 32901
(407) 724-3800
FAX 407-729-5691
Circle No. 717

Hitachi America Ltd
2000 Sierra Point Pkwy
Brisbane, CA 94005
(415) 589-8300
FAX 415-583-4207
Circle No. 718

Lambda Electronics
515 Broad Hollow Rd
Melville, NY 11747
(516) 694-4200
FAX 516-293-0519
Circle No. 719

Linear Technology Corp
1630 McCarthy Blvd
Milpitas, CA 95035
(408) 432-1900
FAX 408-434-0507
Circle No. 720

Maxim Integrated Products
120 San Gabriel Dr
Sunnyvale, CA 94086
(408) 737-7600
FAX 408-737-7194
Circle No. 721

Micro Linear
2092 Concourse Dr
San Jose, CA 95131
(408) 433-5200
TLX 275906
Circle No. 722

Motorola Inc
7402 S Price Rd
Tempe, AZ 85283
(602) 897-3840
FAX 602-897-3392
Circle No. 723

National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95052
(408) 721-5000
FAX 408-245-9655
Circle No. 724

Raytheon Semiconductor
350 Ellis St
Mountain View, CA 94039
(415) 968-9211
FAX 415-966-7620
Circle No. 725

SGS-Thomson Microelectronics
1000 E Bell Rd
Phoenix, AZ 85022
(602) 867-6241
FAX 602-867-6290
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Siemens AG
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Munchen 2, W Germany
(089) 234-3085
FAX 089-234-2824
Circle No. 727

Siemens Components Inc
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Santa Clara, CA 95064
(408) 980-7939
FAX 408-980-4596
Circle No. 728

Silicon General
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Garden Grove, CA 92461
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Applied Microsystems Corporation

Switch-mode power-supply ICs

ing CMOS devices, with low internal dissipation—some low enough to qualify as micropower devices—are tailor-made for creating regulated voltages from batteries.

The value is outstanding

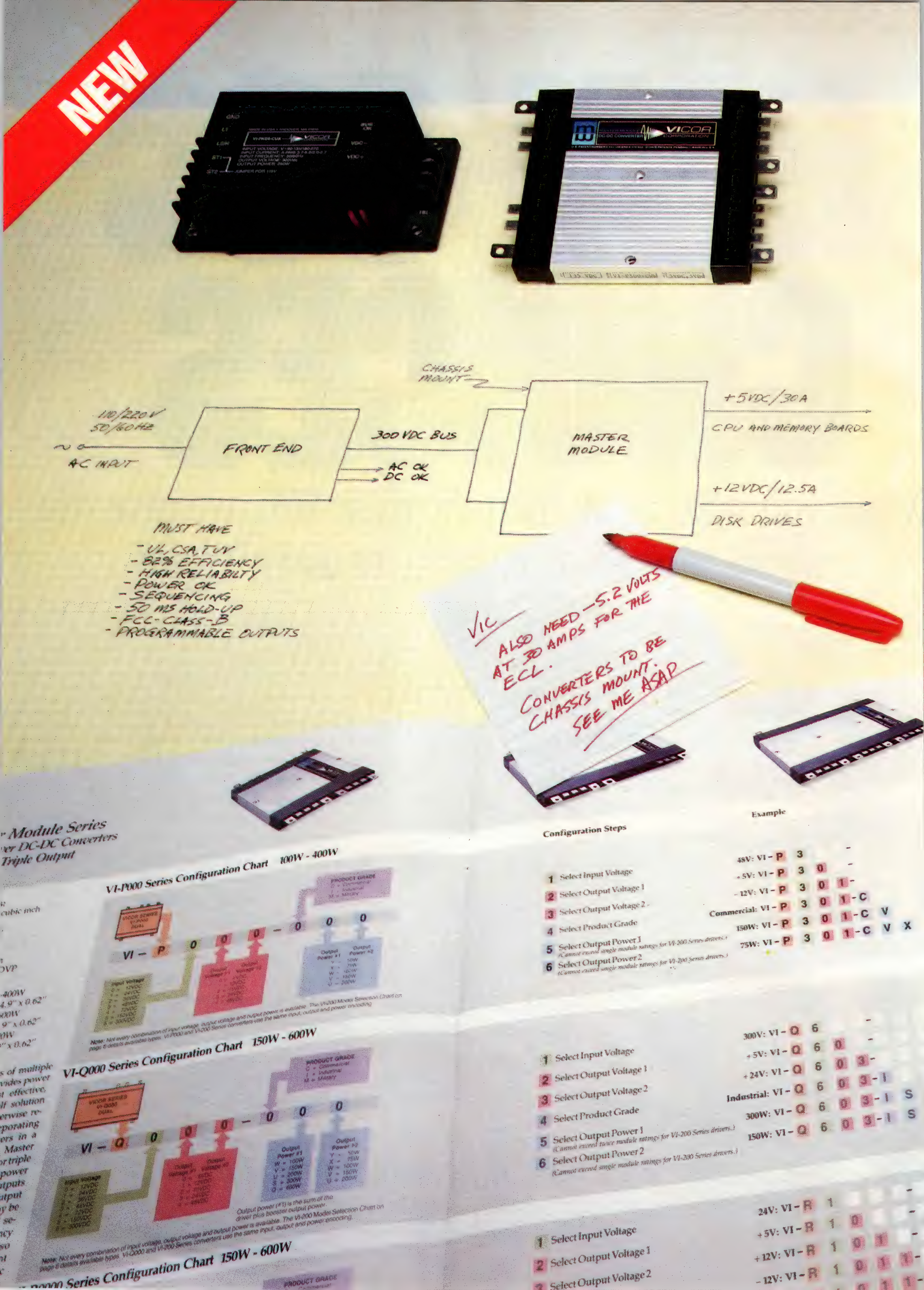
Although there are exceptions, switch-mode power-supply ICs have become commodity parts. The popular types have several sources and pricing is quite competitive, with some parts available in quantity for under \$1 and many more from \$1 to \$2.50. Though the devices aren't as sophisticated as a µP that contains millions of transistors, when you include the combination of analog and digital circuits and the protection features, the value is outstanding.

However, don't let the value and apparent ease of application become siren songs that entice you into attempting to save your company money by building supplies. If you and your company lack experience in designing and building power supplies, you should make any decision to build switchers—especially small quantities of switchers—very carefully. EDN

References

1. Sykes, Frederick E, "Resonant-mode design techniques improve switcher performance," *EDN*, November 9, 1989, pg 201.
2. Sykes, F E, "Resonant converters team control theory and circuit design," *EDN*, November 23, 1989, pg 207.

Article Interest Quotient
(Circle One)
High 518 Medium 519 Low 520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Module Series
DC-DC Converters
Triple Output
VI-P000 Series Configuration Chart 100W - 400W
VI-Q000 Series Configuration Chart 150W - 600W
Configuration Steps
Example
1 Select Input Voltage
2 Select Output Voltage 1
3 Select Output Voltage 2
4 Select Product Grade
5 Select Output Power 1
6 Select Output Power 2
48V: VI - P 3
+5V: VI - P 3 0
-12V: VI - P 3 0 1
Commercial: VI - P 3 0 1 - C
150W: VI - P 3 0 1 - C V
75W: VI - P 3 0 1 - C V X
300V: VI - Q 6
+5V: VI - Q 6 0
+24V: VI - Q 6 0 3
Industrial: VI - Q 6 0 3 - I
300W: VI - Q 6 0 3 - I S
150W: VI - Q 6 0 3 - I S
24V: VI - R 1
+5V: VI - R 1 0
+12V: VI - R 1 0 1
-12V: VI - R 1 0 1 1

OFF-LINE

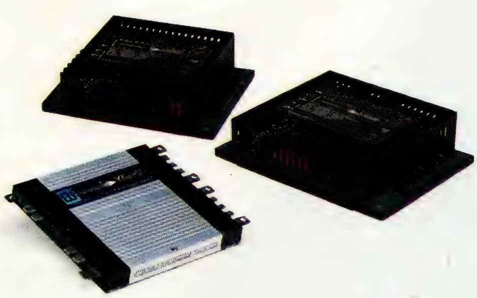
Chassis-Mount Modular Power From 50 to 600 Watts!

In single or multiple output applications, Vicor's family of chassis-mount, power building blocks provide flexible and predictable solutions to virtually any power system requirement.

Vicor's family of chassis-mount, off-line front ends, combined with the Mega and Master Module families of chassis-mount DC-DC converters, allow the power system architect to quickly and predictably customize expandable single or multiple output power systems with output power from watts to kilowatts. Modular power building blocks get you up and running in less time, at less cost, while Vicor's unprecedented levels of power density and efficiency result in less wasted space and heat.

Off-Line Front Ends

Chassis-mount front ends are available in output power ratings of 250, 500, and 750 watts and are designed for direct connection with Vicor's Mega Module and Master Module Series of DC/DC converter modules.



FRONT END SELECTION CHART

MODEL	OUTPUT POWER 250W	500W	750W
VI-FKE6-CUX	✓		
VI-FKE6-CQX		✓	
VI-FKE6-CMX			✓

OPERATING PARAMETERS (ALL MODELS)

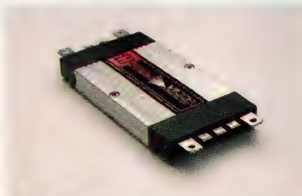
NOM	INPUT VOLTAGE (VAC) LOW	HIGH	TRANSIENT (1 SEC)
110	90	135	150
220	180	270	300

Strappable to provide operation from 90 VAC to 270 VAC lines, the front ends feature conducted EMI/RFI filtering to VDE/FCC A & B, 50 msec holdup, active in-rush limiting and a BUS-OK status output. An opto-isolated AC-OK output is provided for advance warning of DC BUS dropout due to AC line failure.

DC/DC Converter Modules

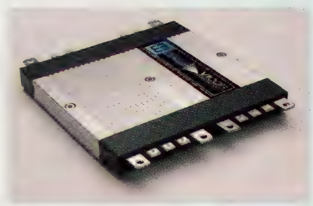
Vicor's Mega Module and Master Module Series of single and multiple output DC-DC converters provide the power system designer with a cost effective, high performance, off-the-shelf solution for applications that might otherwise require a custom supply. These modules incorporate standard VI-200 Series converters in a rugged, chassis-mount package.

Single Output



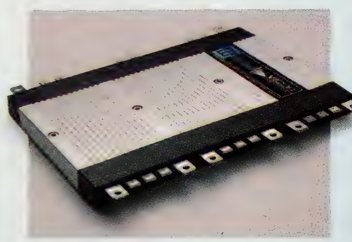
- Single output available from 50 to 200 watts.
- 2.5" x 4.9" x 0.62".

Single and Dual Outputs



- Single output available from 100 to 400 watts
- Dual outputs from 50 to 200 watts each
- 4.9" x 4.9" x 0.62".

Single, Dual and Triple Outputs



- Single output available from 150 to 600 watts.
- Dual outputs with the first output from 100 to 400 watts, and the second output from 50 to 200 watts.
- Triple outputs from 50 to 200 watts each.
- 7.3" x 4.9" x 0.62".

Specify your configuration by picking any combination of Vicor's standard output voltages (5, 12, 15, 24, 48 VDC) at the power levels you need. Vicor does the rest. If standard output voltages don't meet your needs, Vicor can provide semi-custom outputs anywhere in the range of 2 to 100 VDC! For complete details and applications information, please refer to the Mega Module and Master Module sections of the Vicor Product Catalog.

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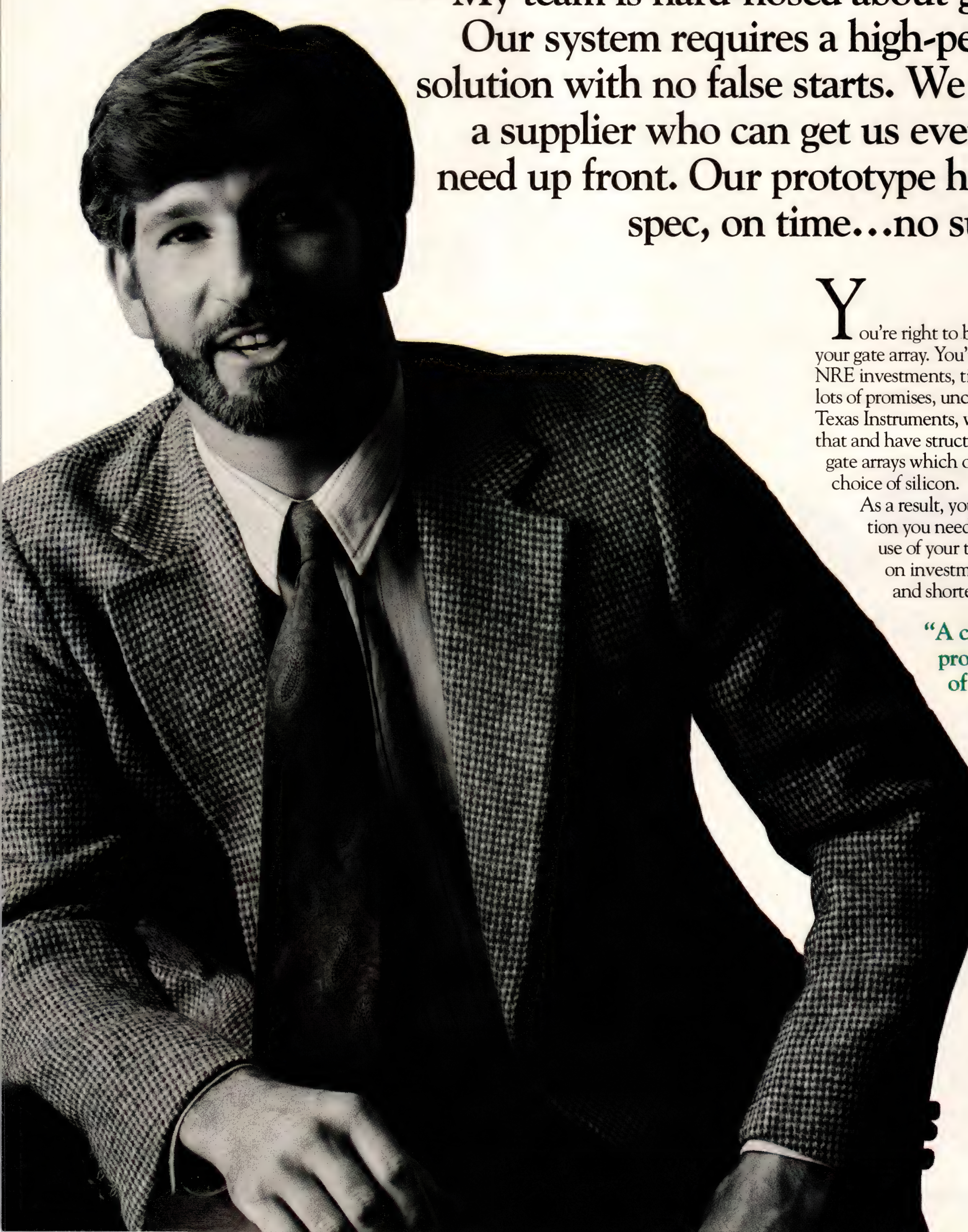
Component Solutions For Your Power System

IN THE ERA OF MegaChip™ TECHNOLOGIES

ASIC SOLUTIONS

"My team is hard-nosed about gate array Our system requires a high-performanc solution with no false starts. We must hav a supplier who can get us everything w need up front. Our prototype has to be o spec, on time...no surprises.



You're right to be hard-nosed about your gate array. You're a veteran of high NRE investments, tight market windows lots of promises, uncertain results. At Texas Instruments, we have anticipated that and have structured an approach to gate arrays which offers you more than a choice of silicon.

As a result, you not only get the sol tion you need, but you make bette use of your time, improve return on investment, lessen the risks, and shorten the design cycle.

"A clear-cut design process with plenty of support is a necessity."

TI's design flow is very straightfor- ward. Areas of control are defined to mir mize the pos- sibility of surprises. Our goal is the sam as yours — a shortened design cycle time. When necessary our design flow ca be adapted even more precisely to fit your needs.

GATE ARRAYS

TI's service and support are comprehensive — and available to you from Texas to Taiwan. Among the highlights:

Our TGC100 Series Design Kit, operating on Daisy/Cadnetix (DAZIX™), Mentor Graphics™, and Valid™ workstations, provides the necessary information to easily implement your gate-array design.

Person-to-person advice and counsel are provided worldwide by ASIC applications specialists in our field sales offices. ASIC design specialists are stationed at ASIC design centers in our Regional Technology Centers, where our design workshop is also conducted regularly.

Delivery schedules can be tailored to support your ship-to-stock or just-in-time programs anywhere in the world.

"We demand high performance in our arrays."

The TGC100 arrays are fabricated in TI's 1-micron EPIC™ CMOS process technology. Typical gate delays are 500 ps with flip-flop toggle rates up to 208 MHz.

"We prefer a choice of densities plus design options."

TI's TGC100 arrays range in complexity up to 26K gates. You call the shots on pin count, pinout definition, and the package itself by choosing from our variety of packages having pin counts up to 256 pins (*see table below*).

TI's gate-array library contains more than 200 macros, many essential to attaining high-performance designs. For example, a clock distribution macro minimizes clock skew. Input/output buffer macros minimize unwanted voltage transients and drive heavy capacitive loads.

In support of the JTAG standard, SCOPE™ macros permit incorporation of design-for-test features.

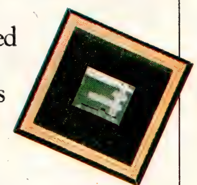
A path-length criticality parameter allows you to specify the delays on critical nets. This acts to minimize the physical length of the interconnect traces and reduce overall propagation delay.

When you have more demanding requirements, the following options give you maximum flexibility in achieving the exact gate array you need:

- Additional prototypes
- Additional 1-MHz test vectors
- Prototype devices tested over temperature and V_{CC} ranges plus DC parametrics
- Critical-path delay measurements (pin-to-pin)
- "At speed" test vectors
- Nonstandard V_{CC} and ground-pin locations
- Operating temperature range other than $0^{\circ}C$ to $70^{\circ}C$

Tomorrow's outlook

Just as our TGC100 Series gate arrays meet the majority of your needs today, our gate arrays of tomorrow will fill the predominant industry needs for submicron densities.



Already, TI has disclosed an array having 106K gates, fabricated with TI's EPIC-II, 0.8-micron BiCMOS technology. High density combines with high performance — ECL speeds at CMOS power levels. This technology is the foundation for an entire family of submicron ASIC products from TI.

For more information on TI gate arrays, call, fax, or write us. **In Europe** call 44-234-223000, fax 44-234-223459, or write Customer Response Centre, MS 09, Texas Instruments Limited, Manton Lane, Bedford MK41 7PA, England. **In Japan** call 81-3-769-8700, fax 81-3-457-6777, or write Texas Instruments Japan Limited, MS Shibaura Building 9F, 4-13-23 Shibaura, Minato-Ku, Tokyo 108, Japan. **In Hong Kong** call 852-735-1223, fax 852-735-4954, or write Texas Instruments Hong Kong Limited, Market Communications Department, 8th Floor World Shipping Centre, 7 Canton Road, Kowloon, Hong Kong.

TI's TGC100 SERIES COMMERCIAL GATE ARRAYS

				PRODUCTION PACKAGE OPTIONS																				
				PLASTIC DIP		PLASTIC LEADED CHIP CARRIER				PLASTIC QUAD-FLAT PACKAGE*								PLASTIC PIN-GRID ARRAY						
GATE-ARRAY TYPE	TOTAL CELLS	MAXIMUM USABLE (90%)	TOTAL BOND PADS	28	40	28	44	68	84	80	100	120	132	144	160	208	240	100	120	132	144	180	208	256
TGC104	3,600	3,240	100	X	X	X	X	X	X	•	+•							X						
TGC105A	4,500	4,050																						
TGC106	5,600	5,040	130	X	X		X	X	X	•	+•	•	+					X	X	X				
TGC107	6,720	6,048																						
TGC108A	8,340	7,506	158	X	X		X	X	X	•	+•	•	+	•	•			X	X	X	X	X		
TGC110	10,008	9,007																						
TGC113	12,654	11,389	196					X	X			•	+	•	•	•		X	X	X	X	X	X	
TGC115A	14,706	13,235																						
TGC116	15,580	14,022	216									•	+	•	•	•	•			X	X	X	X	X
TGC119	18,620	16,758																						
TGC122	21,854	19,669	256												•	•	•					X	X	X
TGC126	25,868	23,281																						

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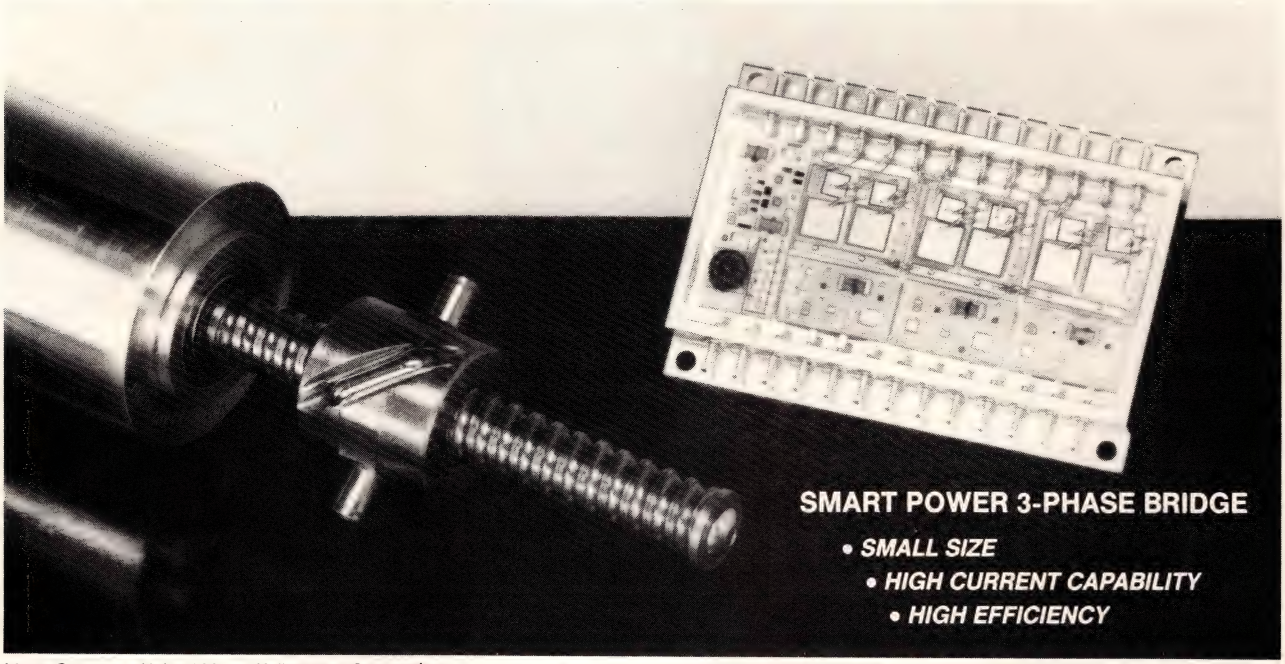
WE'RE CHANGING THE WAY THE WORLD LOOKS AT MOTOR DRIVERS



Motor Courtesy of Inland Motor, Kollmorgen Corporation.

That's right! The world is changing with the introduction of the PWR-82331, DDC's new family of motor drive products.

The PWR-82331 30A, 200V, 3-Phase bridge power hybrid consists of six N-channel power MOSFETS and six anti-parallel fast recovery diodes connected into a full 3-Phase bridge driver. Each MOSFET bridge is driven directly from a CMOS input through high and low side drivers without the need for external bias voltages.

Internal protection circuitry prevents in-line transistors from simultaneous conduction and eliminates multiple upper or lower conduction. A constant voltage drive to control the MOSFETS is used to ensure uninterrupted performance of the drivers even in a motor stall situation—performance that cannot be achieved when a boot-strap configuration is utilized.

The PWR-82331 has its own built-in power source which supplies all the required internal biasing and logic supplies. The Vb input to the internal supply can either be hooked directly to the Vcc pin or to an additional external power source.

This highly efficient bridge uses all N-channel MOSFETS to ensure a very low on-resistance of 0.11 Ohm per leg and 50ns fast recovery power rectifiers to clamp inductive flyback. The PWR-82331 is packaged in a thermally efficient copper case with a typical junction-case thermal resistance of 0.5° C/W and measures only 2.1″W x 3.0″L x 0.375″H. This hybrid is designed to operate from –55° C to +125° C, and is fully processed to MIL-STD-883C.

The PWR-82331 can be driven directly from the commutating logic and when combined with a pulse width modulator creates a Servo Motor Controller, which after proper derating, can drive motors up to 6 hp over the full MIL temperature range.

In addition to the PWR-82331, DDC has introduced the PWR-82333 which can handle a 600V Vcc. Also available are the PWR-82340 and PWR-82342 which are 2-phase bridges in an H configuration.

For additional product and application information, contact Bob Fryer at 516-563-5390, or contact the DDC office nearest you. □

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THERMAL-ANALYSIS SOFTWARE

Thermal images provide reliability clues

Thermal analysis, long familiar to mechanical and reliability engineers, can prevent serious thermal problems. Newer thermal-analysis software, tailored to EEs, can help you pinpoint problems while you can still easily fix them.

Anne Watson Swager,
Associate Editor

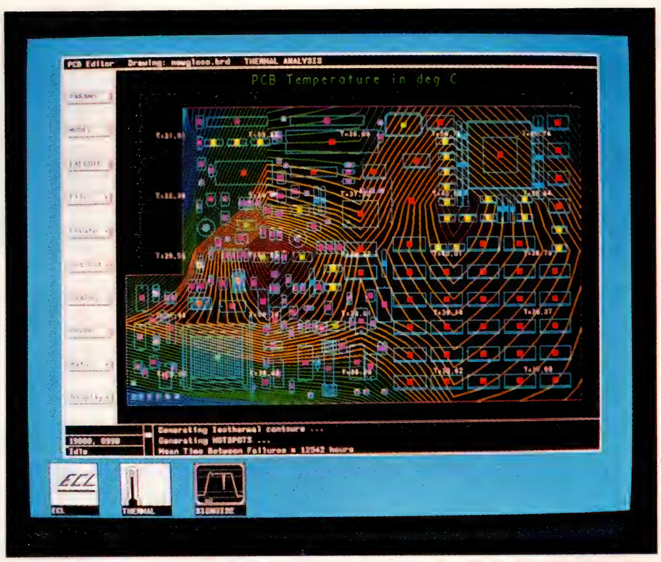
An electronic listening device sitting inside a buoy on the Pacific Ocean, a pacemaker in a human heart, and a missile's guidance system are products that can't tolerate unreliability. And reliable product performance is what thermal analysis helps to ensure. Thermal analysis is especially critical for those products that aren't easily serviced, require the utmost in safety, control military equipment, and for designs that are difficult or dangerous to test.

Granted, reliability prediction is tricky. The relationship between temperature and reliability is not determined or fixed. However, you can be sure that if you violate a device's maximum junction temperature, it won't perform very well for very long. Thermal analysis can predict such extreme cases.

Thermal analysis is nothing new to mechanical and reliability engineers. Now, the increasing density of electronic components forces electrical engineers to consider thermal effects early in a design cycle (**Ref 1**). There isn't time to wait for a dedicated reliability engineer to complete an in-depth analysis. If you wait, you lose the whole advantage of thermal analysis—the ability to evaluate and change a design before you actually build it.

Many thermal-analysis tools are now available. In the last few years, electronic CAD and software companies have introduced packages tailored to pc boards, heat sinks, and electronic enclosures. CAD companies link thermal analysis with their pc-board-layout tools and component libraries so that you can simultaneously design your circuit and perform thermal analysis (**Fig 1**).

The fundamental results of a thermal simulation indicate when your design violates an IC's maximum junction temperature or a component's maximum operating temperature. Basically, the programs use thermal-resistance and power-dissipation data to model junctions and resistors as heat sources. All packages provide you with a steady-



***New thermal-analysis programs tailored to pc boards** are available from many CAD vendors. These packages use heat-transfer and fluid-flow equations to solve for steady-state temperatures and in some cases transient temperatures. A common graphical representation displays isotherms, which are lines of constant temperature. (Courtesy Valid Logic.)*

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Thermal-analysis software

state picture of a board's, component's, or object's temperature profile. Some packages also perform transient analysis, which allows you to determine how the temperature changes at start-up. These and other specifications for the packages discussed in this article are listed in **Table 1**.

Before you approach vendors, make sure you have a clear picture of your own objectives. Start by answering a few questions: What types of systems do you want to model? Power transistors mounted on a lone heat sink? A single pc board with components on one side? A board with components on both sides? A whole card cage? A whole enclosure with multiple card cages? Are you well versed in CAE tools, and are you interested in linking the thermal-analysis software with your other tools, such as pc-board-layout tools?

All thermal-analysis software packages solve some set of heat-transfer and fluid-flow equations using a particular numerical scheme. Because each program uses a unique set of equations, comparing different packages is difficult. You may be able to determine a program's accuracy by studying the vendor's test results. Ultimately, the more questions you ask software vendors, the better.

The first criterion for any package you buy is that it accurately models your particular system and produces reliable results. The second most important criterion is how easily thermal analysis inserts into your design flow. In other words, how easy is it for you to implement **Fig 1**'s design scenario? Of course, cost is always a factor, so be sure you consider the total thermal-analysis costs. Some of the programs in **Table 1** require additional packages to process and display the data.

To satisfy the accuracy criterion, you'll need some idea of what's involved in computational heat transfer and fluid dynamics. The numerical technique and set of equations each software package relies upon makes a big difference in the accuracy of your thermal-modeling result. And, the type of numerical scheme that yields the best result depends heavily on the complexity of your model's component geometries. Modeling air flow in an aircraft engine and around a pc board are quite different tasks.

Both finite-element and finite-difference techniques solve heat-transfer and fluid-flow equations using matrix techniques. Finite-element schemes are typically more accurate for complicated geometries; finite-

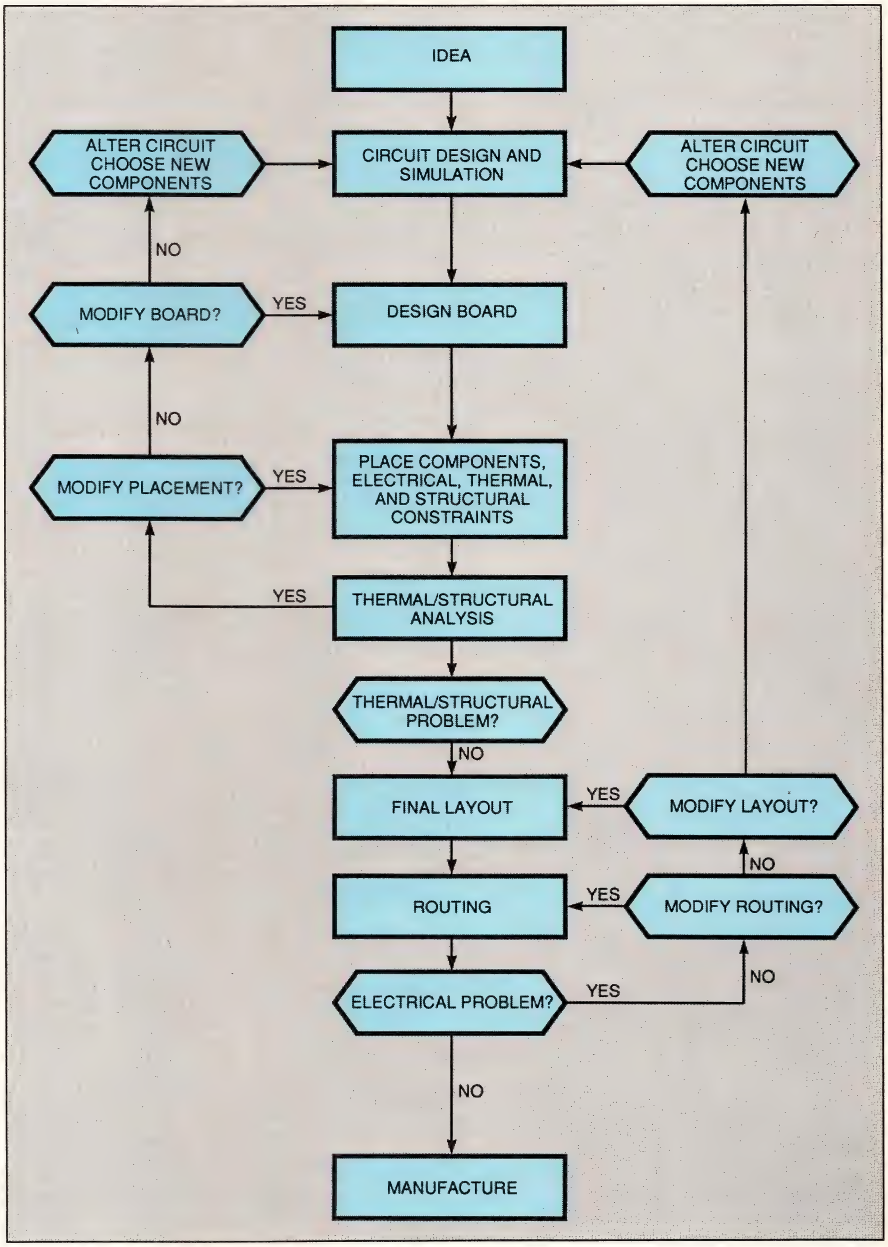


***Fig 1—By integrating thermal analysis** into your circuit's design and layout cycle, you can find thermal problems and make changes before your product's physical design is complete.*

Thermal-analysis software

difference schemes use simpler algorithms and suit regular geometries. As for the software itself, the major difference between the two methods lies in the size of the matrices formed and the solver's iteration scheme. According to Fluid Dynamics, the finite-element technique requires more computer resources per iteration than the finite-difference technique. Thus, it may take more computer power and

Table 1—Representative thermal-analysis software packages

Manufacturer (Distributor)	Software package	Price	Program type	Dimensions modeled	Numerical method	Hardware platform	Transient analysis	Comments
BV Engineering Professional Software	STAP	$125	General purpose	2	Finite difference	IBM PC or compatible, Macintosh		Tailored to heat-sink modeling. Requires Pcplot and Pdp programs to plot and print results. Conduction only.
CAD Software	Pads-thermal	$975 to $4000	pc board	3	Finite difference	IBM PC or compatible		Software integrated with Pads-pcb layout tools. Version of Dynamic Soft Analysis' beta soft-pc.
Compuflo	Flotran	$8000 to $30,000 (annual license fee)	General purpose	2 and 3	Finite element	Workstation to mainframe		Requires mesh-generation software such as I-deas, Patrans, or Ansys.
Daisix	PCB thermal	$20,000	pc board	3	Finite element	Sun's Sparc, 386i, or HP workstation	•	Software includes interface to other pc-board-design tools. Version of Pacific Numerix's PCB thermal.
Dynamic Soft Analysis Inc	Betasoft-pc	$3000	pc board	3	Finite difference	IBM PC or compatible		Latest package upgrade includes reliability calculator.
Flomerics Limited	Flotherm	7500£ to 40,000£ (perpetual license fee) 6000£ to 16,000£ (annual license fee)	General purpose	2 and 3	Finite element	IBM PC or compatible to mainframe	•	Models entire electronic systems and enclosures.
Fluid Dynamics	Fidap	$3000 to $26,000	General purpose	2 and 3	Finite element	Workstation to mainframe	•	Includes mesh-generator program, Fimesh, and preprocessor program, Fiprep.
Helios (Management Sciences)	Thermax	$4500 to $15,000	pc board	2, 2.5, and 3	Finite difference	IBM PC or compatible, Sun, DEC, or Apollo workstation	•	Interactive, mouse-driven software. Also models radiation effects.
HTRD Software	Tlayers	$1980	General purpose	3	Finite element	IBM PC or compatible		Tailored to IC hybrids, power supplies, and power hybrids. Conduction only.
Intergraph	PCB thermal	$20,000	pc board	3	Finite element	Intergraph workstation	•	Features icon-driven user interface that links the thermal model to other pc-board-design tools. Version of Pacific Numerix's PCB thermal.
Mentor Graphics	Autotherm	$69,000	pc board	2.5	Finite element	Apollo workstation		Price quoted is for the Package Station, which includes Autotherm. Also models radiation effects.
	Prototherm	$14,900	pc board	2.5	Finite element	Apollo workstation		Thermal package is part of the board station. Also models radiation effects.
Pacific Numerix	PCB thermal	$15,000	pc board	3	Finite element	Sun, DEC, or Apollo workstation	•	Thermal software (priced separately) operates within the PCB Design Expert System.
Racal-Redac	Visula thermal	$17,000 to $19,000	pc board	2.5	Finite difference	Sun, DEC, or Apollo workstation	•	Thermal models rely on both theoretical calculations and real measurements of device performance.
Techna/Soft Systems	T/SNAP	$985 (8088 version)	General purpose	3	Finite difference	IBM PC or compatible	•	Tailored to analysis of complex thermal networks. Also models radiation effects.
Valid Logic	Thermostats	$15,000	pc board	2.5	Combined finite element and finite difference	Sun or DEC workstation		Package includes reliability calculator. Also models radiation effects.
Visionics	EE designer III/E	$5995	pc board	3	Not specified	IBM PC or compatible	•	The EE Designer extended version integrates thermal software with other pc-board design tools. Conduction only.

NOTE: All packages model the effects of conduction, and natural and forced convection unless otherwise specified.

Thermal-analysis software

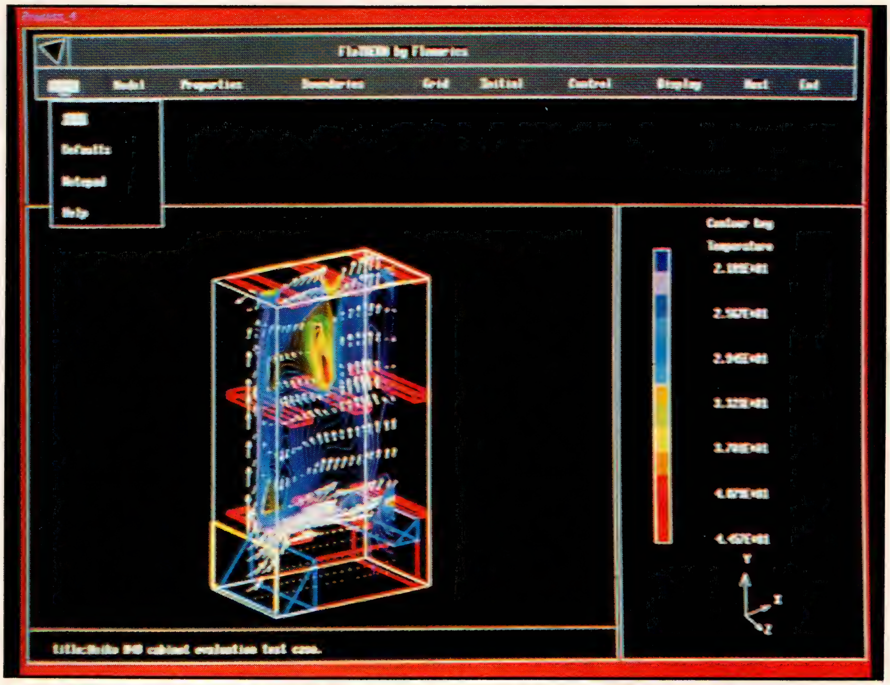
processing time. However, Fluid Dynamics claims that the finite-element technique usually requires fewer iterations to converge on a solution than the finite-difference method.

A main difference between these methods, then, is the issue of convergence and convergence time. Finite-difference schemes sometimes use what some call computer "tricks" to speed the computations and ensure convergence. However, one company's trick is another's unique software solution. The "tricks" basically boil down to the software making assumptions to ensure that the solution will always converge.

Another difference between finite-element and finite-difference programs is in the structure of the mesh, which is simply the geometric arrangement of nodes for which the software calculates junction temperatures. To create models that most closely resemble actual components, many finite-element programs use triangular meshes. Meshes composed of triangular shapes can more easily represent circles and other geometric patterns.

Finite-element-based schemes sometimes allow you to create regions of refined mesh. In other words, there may be parts of your board or system that you expect to be more critical than others. You can create a mesh with nodes closer together in those areas and more spread apart in the noncritical areas. A key to producing refined meshes is what Fluid Dynamics calls transition elements. The mesh can't abruptly change from one density to another, and transition elements smooth the transition.

Alternatively, most finite-difference-based programs use rectangular meshes, which are adequate for many pc-board layouts. However, rectangular meshes can only approximate round shapes such as TO power packages. But, according to Dynamic Soft Analysis, the equations of its and CAD Software's packages can correct for mismatches between the mesh and the actual part, so that the rectangular mesh is not a liability.



Modeling temperature inside an enclosure *or any system with multiple heat sources and fans is much more complicated than analyzing a single pc board. Natural, forced, and mixed convection causes complex turbulent effects, which the software must be able to deal with accurately. (Courtesy Flomerics Limited.)*

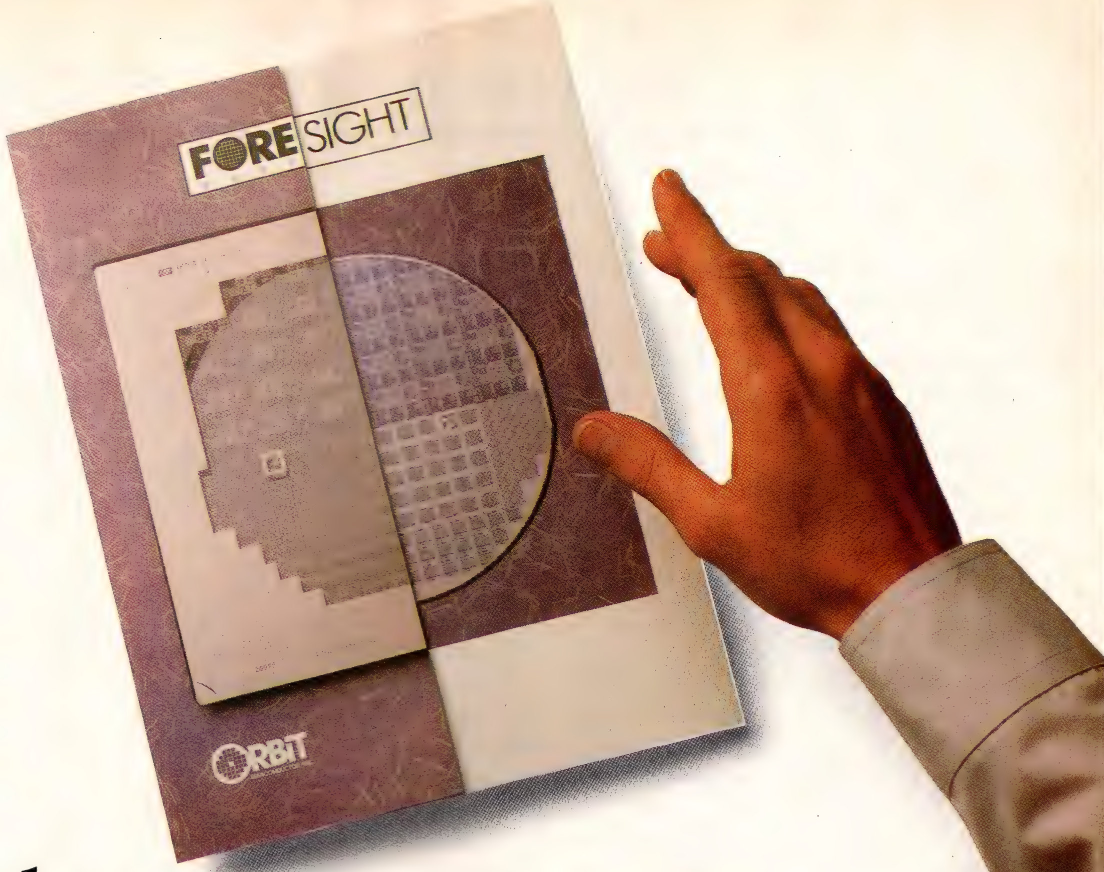
Heat travels in three ways

In addition to numerical schemes and equations, there are heat-transfer and fluid-flow considerations to investigate. All of the software packages model the effects of conduction. A few other packages additionally model convection. Since convection involves molecular motion—a kind of fluid flow—programs that calculate the effects of convection are known as computational-fluid-dynamics programs. And a few others also model electromagnetic radiation.

Modeling conductive effects is relatively straightforward, but thermal analysis gets complicated when you also want to consider convection—especially forced convection. Valid Logic says that an analysis based only on natural convection can often be 99% accurate. However, that accuracy can decrease to 80% with the addition of forced air. High-end packages, such as Fidap, Compuflo, and Flotherm, have elaborate schemes that calculate the effects of turbulent air flow.

Yet another feature you should investigate is the number of dimensions that the software actually simulates. Some packages model in 2-D, 3-D, and even 2.5-D. Vendors use the term 2.5-D to refer to models that aren't purely 3-D, but model more effects than purely 2-D systems.

Two-dimensional software makes one major assumption: the board or substrate thickness is so thin compared with its surface area that its effects are negligible. More specifically, the temperature through the thickness of the board is uniform.



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Thermal-analysis software

Three-dimensional modeling takes all board layers into account, so that you can determine temperatures at each multilayer surface. The definition of 2.5-D is by no means standard. Thermostats, a 2.5-D analyzer from Valid Logic, neglects component height but does account for multiple board layer temperatures.

Mentor Graphics' scheme is substantially different from Valid's. Mentor's Autotherm transforms a 3-D model into a 2.5-D model (**Fig 2**). The 3-D model includes all the thermal resistances from the semiconductor junction to ambient air and from the junction to the pc board, and it models the junction itself as the heat source, Q_V. Autotherm transforms the extended model into a simpler model by modifying the power and combining the thermal resistances. According to Mentor, these modifications ensure that the board-surface temperature and the heat flow into the pc board are both completely accurate. Thermax, from Helios, is another program that models so-called 2.5-D effects. The package, an enhanced version of the company's 2-D package, analyzes the effect of air flow over and under a pc board.

Obviously, you'd want to use a 3-D program if you plan to model, for example, a thick block of material. And many CAD vendors say that 3-D is important for pc boards as well, especially when they have multiple layers and components mounted on both sides. Many of the programs in **Table 1** are available in both 2-D and 3-D versions.

Take the right steps

Once you've compared various packages' accuracy, you can examine other features that determine how easy the software is to use. Each thermal-analysis package includes many other features that accomplish the basic steps of any thermal-modeling problem (**Fig 3**). These steps are common to all software programs, but each is implemented in different ways. Many of the steps are automatic. You have to perform other steps manually, or provide additional information to the program.

Software available from CAD vendors who also provide pc-board-layout tools performs the first three steps shown in **Fig 3** virtually automatically. During the pc-board-layout stage, you've already essentially defined the entire geometry, and with this information the software automatically creates the mesh. The library you use at the layout stage includes thermal data about the component either in the component's library or a separate thermal library. For example, Mentor's Autotherm extracts board geometry and component placement directly from the company's board-station data. The company's Package Station parts library includes thermal properties such as resistivity, conductivity, and power dis-

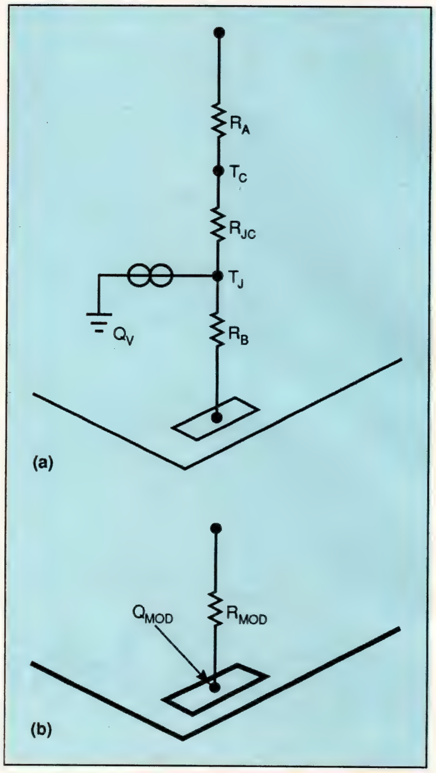
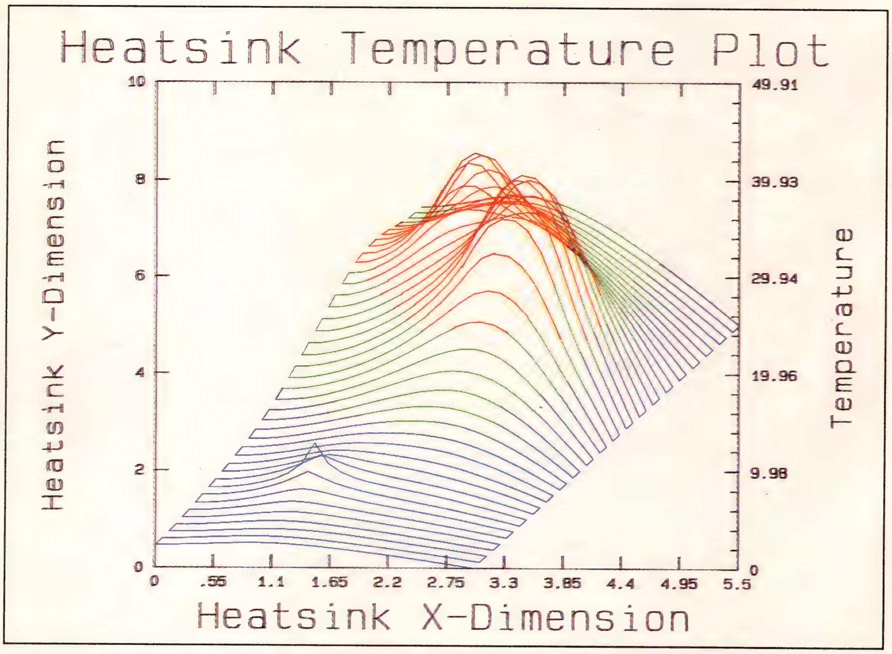


*Fig 2—**Software packages that model 2.5 dimensions** include 3-D effects in an essentially 2-D analysis. Mentor Graphics' Autotherm package transforms a 3-D model, **(a)**, into its 2.5-D model, **(b)**, by modifying the power and combining the thermal resistances.*



***Two-dimensional software can model simple systems** such as 20 transistors and components mounted on a single heat sink. (Courtesy BV Engineering Professional Software.)*

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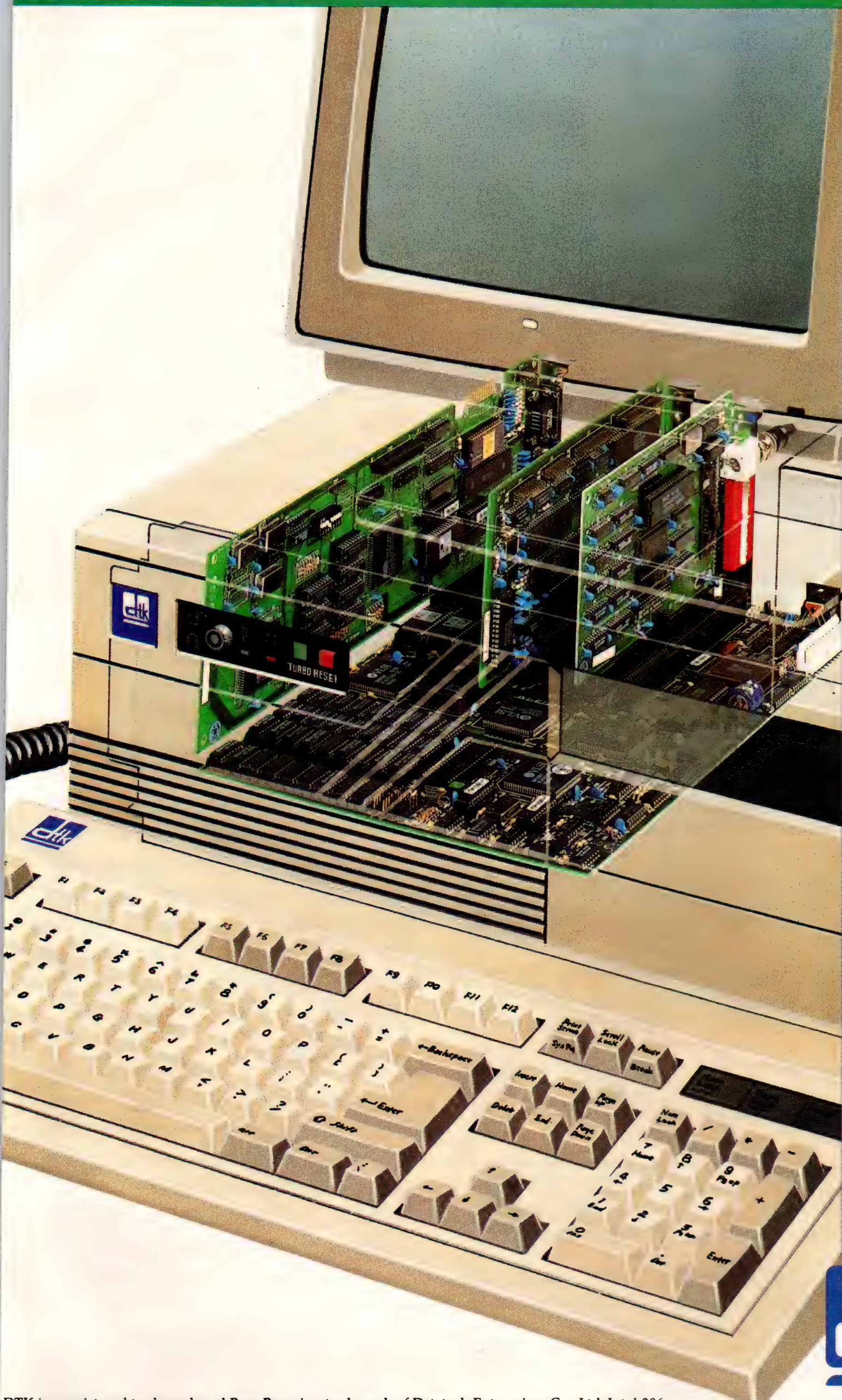

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The one exception to this automatic process occurs when a component doesn't appear in the vendor's library. All software vendors provide a way for you to define additional components, but you must supply all thermal data. Obtaining this information may not be so simple. In many cases, semiconductor manufacturers have supplied CAD vendors with data that isn't available on a part's data sheet. For example, Bipolar Integrated Technology (Beaverton, OR) supplied all mechanical and thermal data about its parts directly to Valid so that Valid could include the parts in their library. Also, CAD vendors may have done some testing of their own, and refined their own models. For example, Mentor creates some of its own equivalent models from IC material and die-size information.

To obtain thermal data, which is in many cases not printed on data sheets, you may have to contact manufacturers yourself; however, don't expect them to have all the data you want. If you do get a hold of some data, you need to be quite confident of its validity. Also, some specifications may produce results more erroneous than others. According to Valid, incorrect power-dissipation information is a major source of analysis error.

Examine the libraries

To date, you'll find that all vendors have standard components in their libraries, such as resistors, capacitors, and digital ICs in both TTL and CMOS. Most libraries also include a variety of package styles, such as DIPs and surface mount, and some include TO power packages. However, you can safely assume that any unique component—a high-speed, wide-bandwidth op amp or a power amplifier—will require you to create a new model to accompany it.

If you're using a general-purpose thermal-analysis package that isn't linked to other design tools, the mesh description may involve more work, such as specifying X and Y coordinates, for example. Some packages allow you to define the mesh by specifying fine or coarse points. You may need additional software programs for mesh generation. Compuflo's Flotran, a high-end program, requires additional software such as Ansys and Padtrans, which are more familiar to users of mechanical-CAD software.

Defining boundary conditions essentially amounts to giving the program certain constraints on ambient temperature, temperatures of any card guides that make contact with the pc board, and air velocities (if your system has a fan). Depending on the package, you may also have to specify heat-transfer and convection coefficients at this stage.

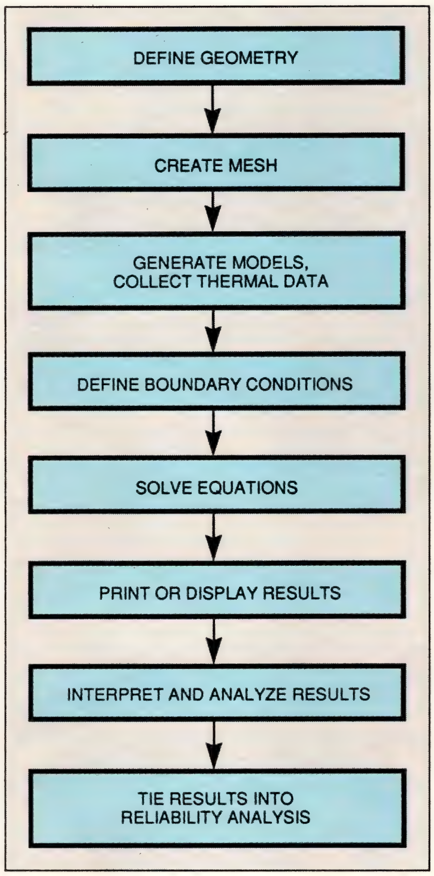

*Fig 3—**Some of these basic thermal-analysis steps** can occur automatically; others may require additional software or more information from you. The last two steps require you to make decisions about temperature effects and reliability.*

The time required for the next step, solving the equations, can vary tremendously. Depending on your package's numerical scheme, the complexity of your models, the density of the mesh, and the computer you're using, solutions can take anywhere from minutes to hours. Some vendors quote typical simulation times on their brochures. For example, Betasoft-pc and Pads Thermal have typical computation times of 2.5 minutes for a board of 100 components running on an IBM PC/AT with a math coprocessor.

Each vendor uses a variety of methods to display the results. Many packages display isotherms, which are lines of constant temperature. Some packages allow you to zoom in to a particular component to determine its junction temperature. You can plot data and also get a simple listing of temperatures (one of the less useful outputs).

You must interpret and analyze the results, and then make the corresponding design changes. Although some CAD system's layout tools can make simple changes based on thermal results, the design engineer is the best person to oversee such layout changes. You wouldn't want the software to arbitrarily move a component based only on temperature considerations when that component also is part of a sensitive signal path.

Obviously, temperatures that exceed a component's maximum ratings necessitate design changes. But marginal temperatures may or may not lead to component failure. In an attempt to quantify the temperature-reliability relationship,

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Thermal-analysis software

Valid's Thermostats and Dynamic Soft Analysis' Betasoft-pc incorporate reliability calculators into their packages. The software uses MIL-HDBK-217 criteria to calculate MTBF. After each analysis run, Thermostats automatically calculates and displays MTBF.

If you believe the military handbook, such reliability calculations can be revealing. For example, the results of a Valid study indicate that a pc board populated with mostly 256k NMOS DRAMs will double in reliability if you reduce the junction temperature from 100 to 90°C. However, the same temperature reduction on a predominately ECL board improved the reliability by only 22 percent. Also, the results of studies conducted by Dynamic Soft Analysis indicate that the components with the lowest reliabilities are *not* necessarily those with the highest junction temperatures.

Regardless of the unknowns of these relationships, vendors who package reliability and thermal analysis together or provide separate reliability packages linked to thermal analysis are on the right track. Although you may only want to use thermal-analysis software to find a pc board's hot spots, the software can give you much more complete information. Armed with that information, you can design your product with much greater assurance that it will perform as reliably as your customers demand it to.

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1. Swager, Anne "Circuit design requires thermal expertise," *EDN*, June 22, 1989, pg 93.

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For more information . . .

For more information on the thermal-analysis software packages discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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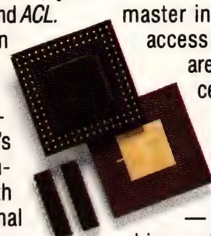

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CIRCLE NO. 38

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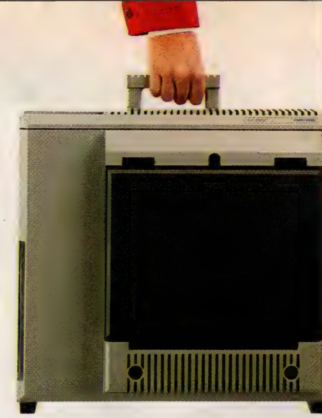


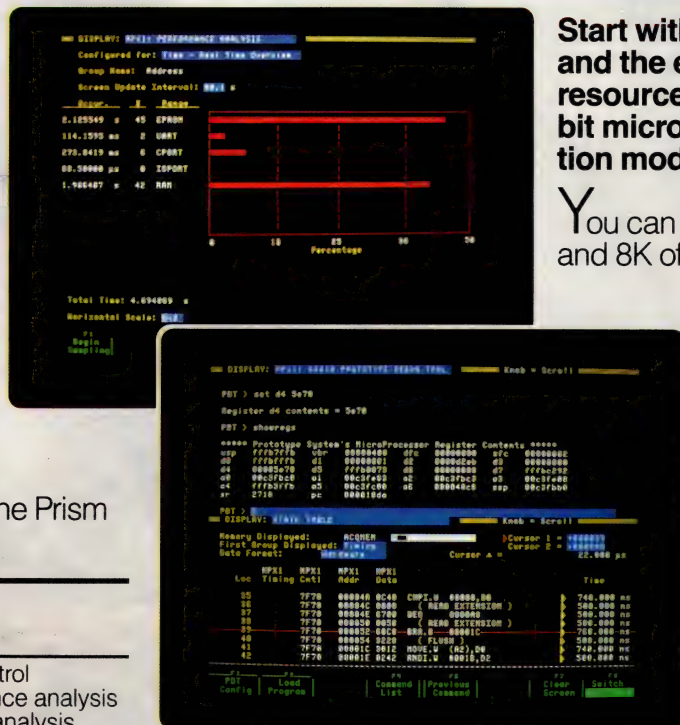
Visualize a logic analyzer that not only acquires microprocessor state and timing data, but adds emulation capabilities... real-time performance analysis... high-speed timing for hardware analysis... and more—all usable in precise, time-correlated combination. All configurable to your needs.

That's the visible edge of the Prism 3000 Series from Tektronix.

The new dimension of integrated analysis.

MPM/MPX Module	Microprocessor control Real-time performance analysis 200 MHz hardware analysis 8K deep state analysis Multiple Microprocessor support
HSM Module	2 GHz hardware analysis 300 MHz state analysis 1.5 ns glitch capture 12K transitionally-stored memory (up to 120K effective memory)

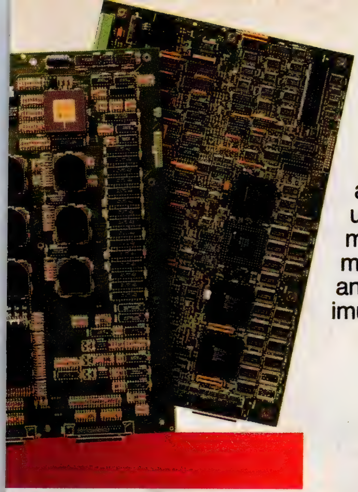
Now, just months after introduction, Prism breaks *new* barriers with a module specifically designed for hardware analysis—for detecting glitches, metastability, and the other common problems of state machines, busses, and sequential logic.



(Above, left) Real-time performance analysis as displayed on the Prism color monitor. (Left) The Prototype Debug Tool provides easy access to microprocessor control and debug functions, including the ability to set hardware and software breakpoints, and to patch registers and memory.

Start with up to 96 channels and the exceptional resources of Prism's 8/16/32-bit microprocessor integration modules.

You can view 200 MHz timing and 8K of state data per channel,



(Left) Prism microprocessor and hardware analysis modules are user-installable in minutes. These application modules can be configured in any combination, up to a maximum of ten cards per system.

all time-correlated and integrated on the same display. Set up state and timing sections to cross-trigger, synchronize and arm each other, so you know exactly when and in what time relationship events occur.

Push beyond microprocessor observation into microprocessor *control*.

With its unprecedented Prototype Debug Tool, Prism lets you easily set breakpoints, patch registers and memory, restart the system —all without an emulator's intrusiveness.

Use real-time performance analysis to get a true, non-statistical view of system performance.

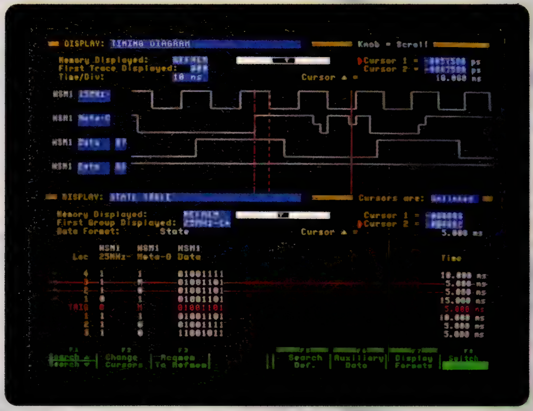
Designers of embedded control systems will especially benefit from histograms of uncompromising accuracy.

Now, with Prism's HSM high-speed hardware analysis module, you can add capabilities like 2 GHz timing and 300 MHz state analysis—and use these tools in tight time-correlation with other Prism modules.

Detect race conditions, setup and hold time violations, and glitches as small as 1.5 ns. Switch to dual threshold or digitizing modes to get a quick look at intermittent problems like ringing or undershoot.

Memory constraints are virtually eliminated: the HSM's 12K of transitionally-stored memory offers the equivalent of as much as 120K of conventional memory!

(Below) The Prism HSM's dual threshold mode triggers on and displays a metastable condition. Middle thresholds are displayed as "M" in the time-correlated state table. Cursors measure the setup time violation that caused the metastable state.



Choose from a stand-alone Prism, expandable mainframe-and-monitor, even a portable model with fold-up flat panel screen.

Features like autoload, split-screen displays, smooth scrolling and on-line help make Prism refreshingly simple to learn and use.

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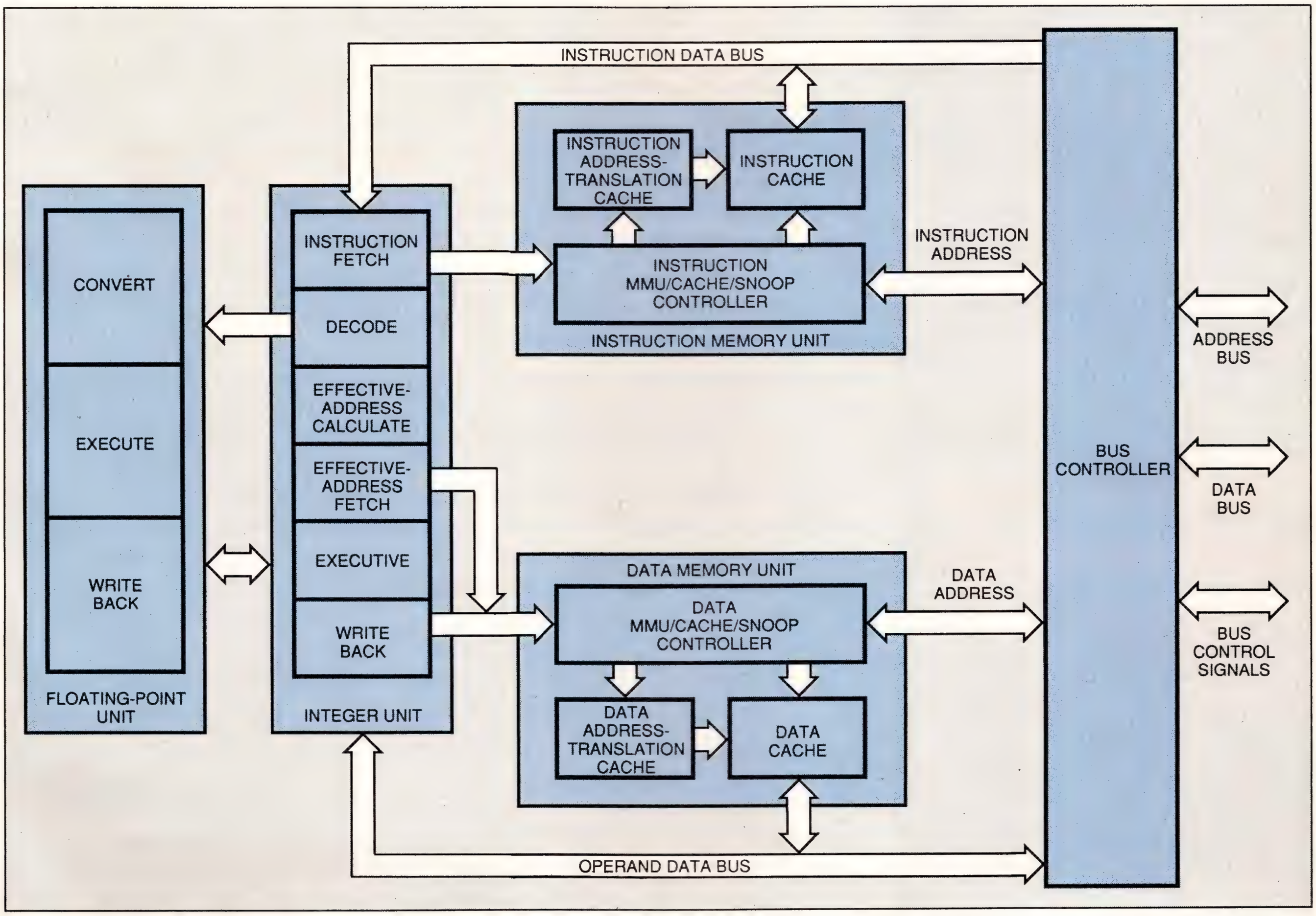
Integral floating-point unit and caches triple 32-bit μP's performance

Marking the processor family's 10th anniversary, the MC68040 μP proves that there's plenty of useful life left in "old-fashioned" CISC (complex instruction set computer) architectures. The new 32-bit μP takes advantage of today's million-plus IC transistor budgets to add hardware that triples the chip's performance with respect to its immediate predecessor, the MC68030. Although the company uses a host of optimization techniques to achieve the extra speed, an on-chip floating-point unit (FPU), enlarged cache memories, and additional integer-unit hardware are chiefly responsible for the performance gains.

At a clock rate of 25 MHz, the μP's integral FPU performs 3.5M double-precision flops, executes 8M flops under peak conditions, and retains object-code compatibility with the company's MC68882 floating-point coprocessor IC used with earlier 68000 family members. The FPU's dedicated hardware executes the most commonly used floating-point instructions; more complex instructions such as transcendental functions execute through microcoded hardware at a rate that still betters the MC68882's speed. A dedicated 64×8-bit hardware multiplier, dual-ported floating-point registers, and register scoreboarding contribute to the FPU's performance.

To help it optimize the MC68040's integer unit, the company used extensive trace analyses of existing 68000 family code (just as it did with the FPU). The integer unit contains hardware that executes the most commonly used instructions in one clock cycle (thanks to a complex pipeline) so that the hypothetical



***Built with more than 1.2 million** transistors, the MC68040 μP delivers three times the performance of its immediate predecessor, the MC68030, yet remains object-code compatible with all of its ancestors including the decade-old MC68000.*

"average" instruction executes in 1.3 clock cycles. Therefore, this μP approaches the RISC (reduced instruction set computer) processor's ideal of 1 clock cycle/instruction. The company claims that the integer unit can execute approximately 20 MIPS at a clock rate of 25 MHz.

A separate stage in the integer unit's instruction pipeline calculates effective addresses for operand fetches and has been optimized for the most commonly used addressing modes (again determined by trace analyses). In addition, the instruction-prefetch stage fetches both targets of a branch, thus speeding branch performance while maintaining backwards compatibility with older μPs in the family and circumventing the need for a delayed-branch scheme. A write-back stage in the integer unit's pipeline schedules operand writes to memory at a lower priority than operand and instruction fetches. This stage helps prevent performance-robbing pipeline stalls.

Separate 4k-byte, 4-way set-associative instruction and data cache memories help to keep the μP's external-bus traffic to an absolute minimum. Each cache has its own paged memory-management unit (MMU), and each cache has its own 64-entry address-translation cache. Dedicated hardware performs address-table searches, thus minimizing the address-translation overhead. The cache MMUs contain snoop circuitry to maintain cache coherency in multiprocessor systems, and the caches support both write-through and copy-back schemes for maintaining cache coherency with external memory. An on-chip bus controller schedules all bus transactions requested by the execution units and the caches, and can perform burst transfers for cache fills and spills.

With all of these hardware features, the company estimates that the MC68040 provides roughly three times the performance of its immediate predecessor, the MC68030. The MC68040 proves that advancing semiconductor technology can enhance the useful life of existing μP architectures by providing substantial performance improvements while retaining compatibility. Samples of the 25-MHz MC68040 cost $700 to $800.

—Steven H Leibson

Motorola Inc, Microprocessor Products Group, 6501 Cannon Dr W, Austin, TX 78735. Phone (512) 891-2839.

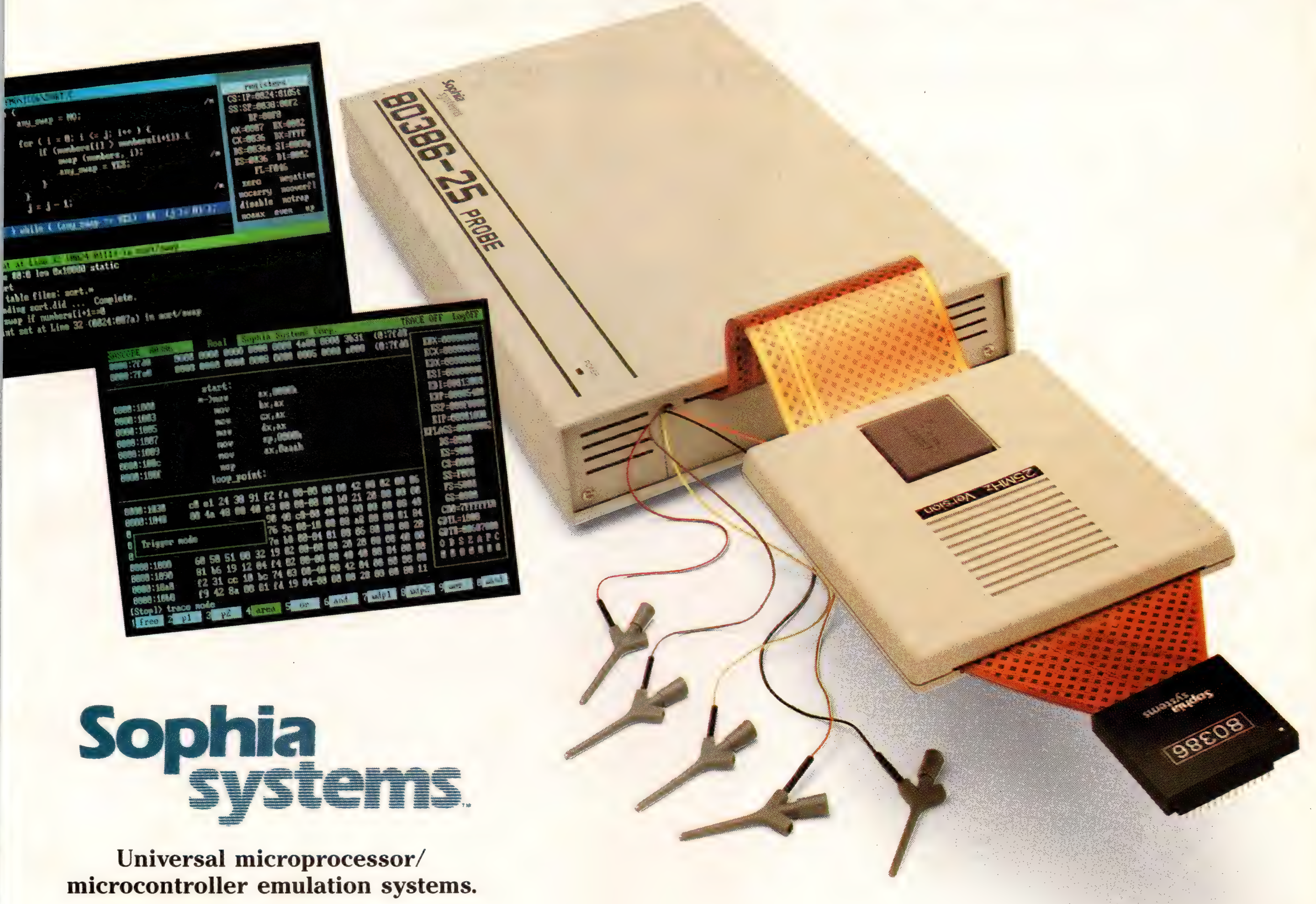
Circle No. 733

Coprocessors by any other name

We call Motorola's MC68882 a coprocessor in this article, and we want to be sure that you know precisely what we mean. At EDN, we have decided to adopt and use standard definitions for the terms "coprocessor" and "auxiliary processor." Michael Slater first proposed these terms in his excellent newsletter, the *Microprocessor Report,* published by MicroDesign Resources Inc, 550 California Ave, Suite 320, Palo Alto, CA 94306, (415) 494-2677.

A coprocessor augments a μP's instruction set with special-purpose instructions (such as floating-point, DSP, or graphics instructions) and fetches its instructions from the same instruction stream as its host processor. An auxiliary processor also supplements the capabilities of a μP, but has its own instruction stream, separate from that of its host. Thus, coprocessors are specifically designed to be mated to the bus of a particular μP or μP family, but any μP can serve as an auxiliary processor.

If you're not interested in second best results...



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Network interface controller simplifies Ethernet for workstations and bridges

If you're designing LAN bridges or including Ethernet in your workstation design, take a look at the DP83932 network interface controller. Dubbed the SONIC (systems oriented network interface controller), this device can simplify your board design and reduce the network's demands on your CPU.

The DP83932 integrates all of the IEEE-802.3 physical-layer options, including layer network management, into a single device that provides a 10M-bit/sec encoder/decoder, media-access control, and transmit-and-receive FIFO buffers. The device's output stage can drive a 50m cable; all you need add is a pulse transformer to make the device meet the Ethernet AUI (attachment unit interface) standard.

You can connect the device to any 16- or 32-bit μP from Intel, Motorola, or National Semiconductor without additional circuitry. The device offers all necessary data, address, interrupt, and bus-access control I/O signals for the various processors. You use a single control pin to select the proper bus-interface characteristics and to handle byte order correctly during data transfer.

The DP83932 can reduce the demand networking places on your CPU. The device's 32-byte transmit-and-receive FIFO buffers allow it to buffer data while waiting for memory access. By using DMA, the device frees the CPU from handling the data.

When receiving a message, the controller stores status and packet pointers in a description area and the data in a buffer area of system memory. When transmitting, the controller can read and send a series of messages from system memory with a single command. The individual messages need not be contiguous or located at set boundaries.

***The DP83932 network interface controller frees your CPU** from the tasks of address decoding and data handling. The controller uses DMA to transfer data to and from system memory and features a content-addressable memory that simplifies address decoding.*

The DP83932 controller provides the logic for slave access and shared-memory control. The logic permits several devices to share buffer space in your system. By using shared memory, you can pass messages between devices without having the CPU create intermediate copies.

The DP83932 also frees the CPU from the task of address recognition. You can program as many as 16 addresses into the device's content-addressable memory (CAM); a broadcast address is preprogrammed. The CAM will signal if an incoming address has a match in its list, thus ensuring that the device will handle only those packets it should.

The addresses you program can be physical (single node) or multicast, thus eliminating the need for a hashing algorithm to handle multiple-destination messages. You can also program the device to accept any message, regardless of address.

The DP83932 operates with system clocks from 8 to 20 MHz and can be used in synchronous or asynchronous systems. The device sells for $55(100).—***Richard A Quinnell***

National Semiconductor, Box 58090, Santa Clara, CA 95052. Phone (408) 721-5000. TWX 910-339-9240.

Circle No. 734

Not-dead-yet CISC workstations fight back

Workstation vendors are engaged in a fierce battle for desktops. The Series 9000 Models 345 and 375 are the latest flurry of punches. Both machines derive their CPU power from a 50-MHz 68030 and a 40-MHz 68882. In addition, you can bulk up the Model 375 with the 68040 through a board upgrade when the new CPU becomes available.

The Model 345 provides 12 MIPS starting at $9000. The system features an optional, 200M-byte SCSI hard disk ($3250). The hard disk comes with the HP-UX operating system and a graphical user interface based on OSF/Motif; both the OS and the interface are preinstalled to allow you to boot the system into a common, user-friendly environment.

To minimize the likelihood of system crashes due to memory parity errors, the system uses ECC (error correction code) RAM. You can configure the Model 345 with 4M to 16M bytes. This low-end system features the HP-HIL (HP's input interface), RS-232C, HP-IB (IEEE 488), Centronics, and IEEE 802.3/Ethernet LAN with thinLAN and AUI (attachment unit interface) as standard interfaces. You can optionally add a SCSI.

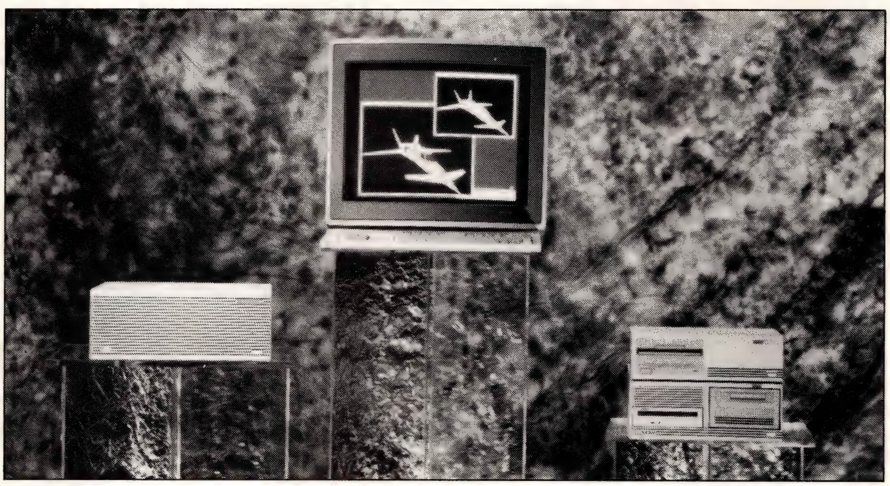
The Model 375 is a 12-MIPS machine that you'll be able to upgrade with a 25-MHz 68040 for $2000 in the second half of 1990. The memory in the Model 375 is also ECC memory; you can configure your system with 8M to 32M bytes of RAM. Later this year, when 4M-bit dynamic RAMs are available, you'll be able to run with 128M bytes of main memory. Unlike the Model 345, the 375 is expandable with 12 I/O slots. Starting at $21,995, the 375 features interfaces equivalent to the 345.

The announcement of the workstations provides HP/UX users with evidence that, contrary to earlier reports, the vendor isn't abandoning the operating system.

—Michael C Markowitz

Hewlett Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No. 735



Compatibile with previous operating systems, *the Series 9000 Models 345 and 375 also provide a path toward the next-generation CPU.*

TEXAS INSTRUMENTS

A PERSPECTIVE ON DESIGN ISSUES:

Beyond VGA

IN THE ERA OF

MegaChip

TECHNOLOGIES

TIGA-340 from Texa

The open graphics interface standar a clear path for your future.

A ground swell of support is rallying behind TIGA-340™, the Texas Instruments Graphics Architecture. It and TI's TMS340 family are poised to become the next standard beyond VGA as PC users demand higher performance and resolution.

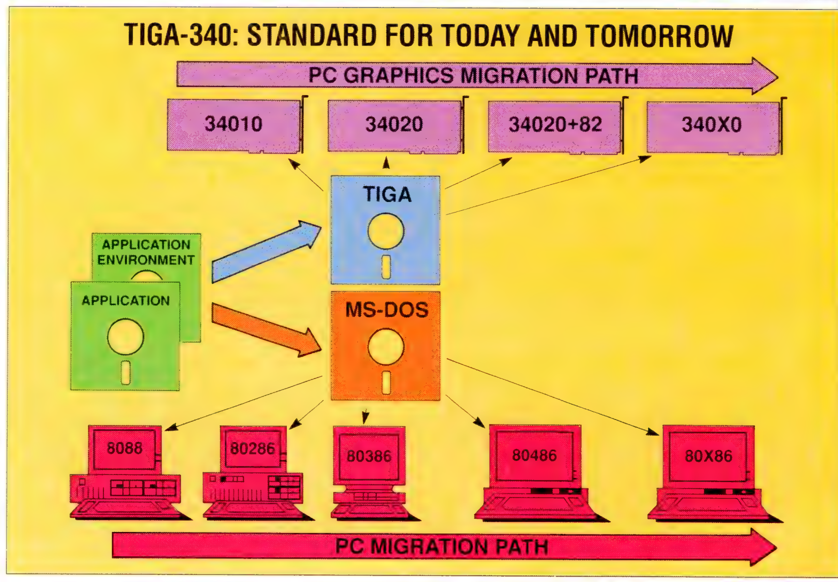
The PC graphics standard anyone can use

TIGA™ is a high-performance software interface that optimizes communications between industry-standard 340 family processors and the PC host processor.

With TIGA, hardware and software specifications for a PC graphics standard are open and available from inception — one of the reasons why more than 100 companies have already made plans to evaluate TIGA-compatible hardware and software products.

Lowest cost, highest performance

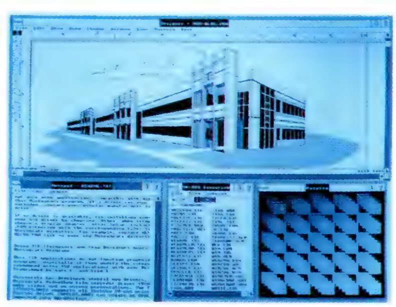
TIGA's move into the mainstream is being fueled by the price of TMS34010-based boards falling to well below $1,000. In fact, TI's 34010 processor is the most economical way to implement high-performance 1024 x 768 resolution PC graphics boards. The faster speed and greater throughput of the second-generation 34020 result in even higher performance boards.



Just as MS-DOS® allows applications to run on any MS-DOS PC using 80X86 processors, TIGA allows graphics applications to run on any TIGA display system using a 340X0 processor.

Clear migration path

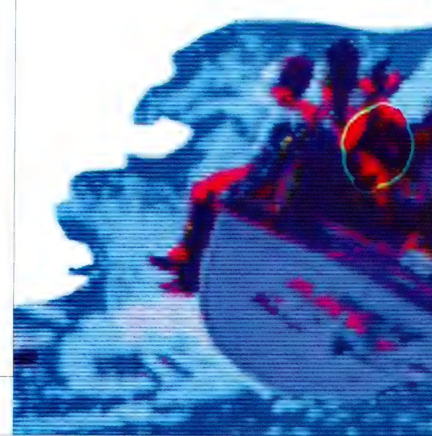
TIGA provides a common platform upon which graphics applications can take advantage of the processing power of the TMS340 family.



Software developers no longer have to rewrite code in order to migrate to higher performance hardware. Software applications that run through TIGA on the 34010 processor run on the upward-compatible 34020 as well as on future 340 family members.

Hardware developers benefit from wide software support, reduced system development time and costs, and easy differentiation of products.

At present, TIGA supports DOS-based PCs, with UNIX™ and OS/2 forthcoming.



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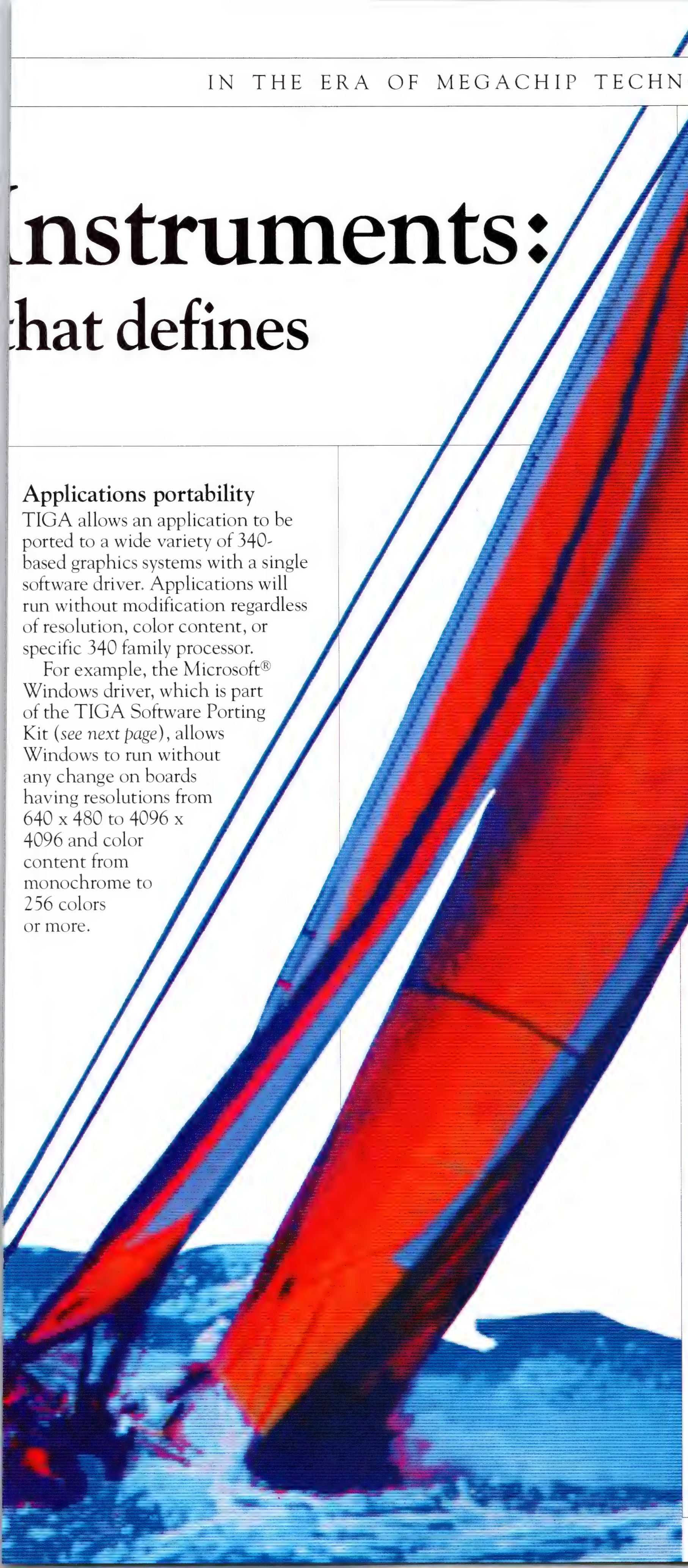


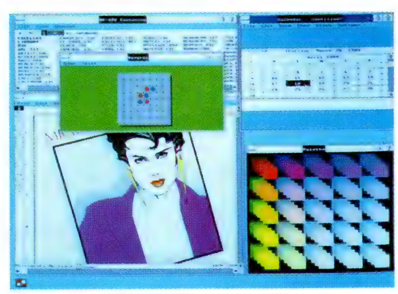
Applications portability

TIGA allows an application to be ported to a wide variety of 340-based graphics systems with a single software driver. Applications will run without modification regardless of resolution, color content, or specific 340 family processor.

For example, the Microsoft® Windows driver, which is part of the TIGA Software Porting Kit (*see next page*), allows Windows to run without any change on boards having resolutions from 640 x 480 to 4096 x 4096 and color content from monochrome to 256 colors or more.

Speeds time to market

Now hundreds of popular applications can be made available for your new graphics product almost instantly using TIGA and Microsoft Windows. Porting TIGA to a 340-based board typically takes less than one man-week of effort.



More than 150 OEMs have made the TMS340 graphics family their own. That wide acceptance, coupled with open architecture and a defined migration path, makes the future for TIGA-340 and the TMS340 family rich and promising.

TI's leadership TMS340 graphics family

No other supplier comes close to TI in the range of cost/performance options for the development of integrated graphics solutions. The widely used TMS34010 processor and other family members are now

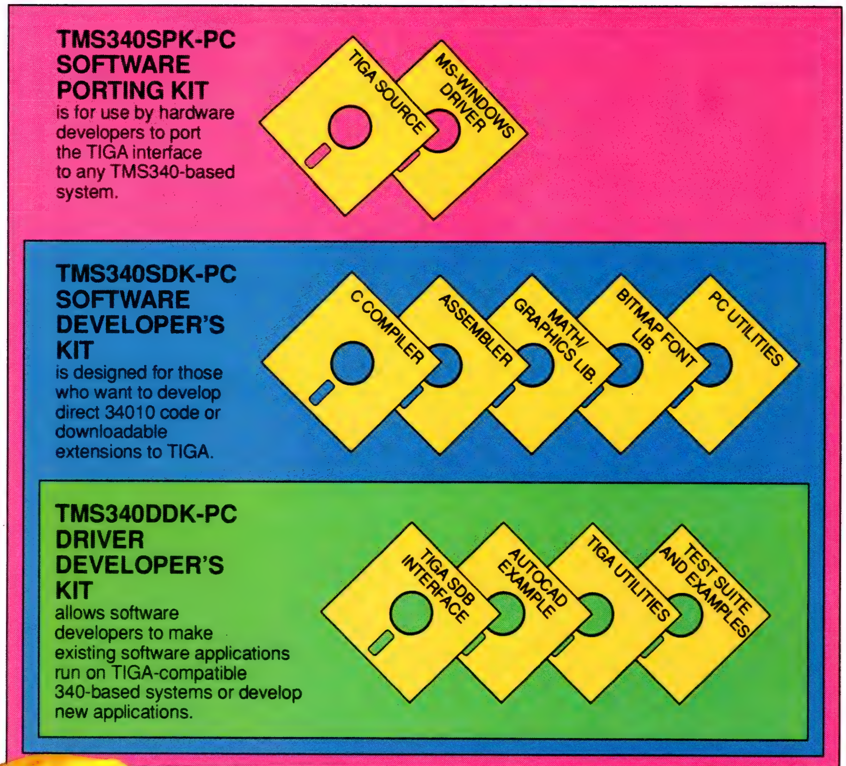
being joined by a group of new-generation products that will bring the higher levels of workstation performance to PCs.

Chief among these is the TMS34020, a programmable, 32-bit processor up to 20 times faster than the 34010.

For use with the 34020, the TMS34082 will perform floating-point operations up to 100 times faster than current PC coprocessors. It is the industry's first graphics floating-point coprocessor.

The family's video RAMs, invented by TI, have been augmented by the TMS44C251 1-megabit VRAM. It was designed in conjunction with the 34020 for the high system bandwidths demanded by today's mid- and high-resolution graphics systems.

TIGA-340 DEVELOPMENT KITS



Free user's guide

For more information about the TIGA-340 standard, get your free copy of the *TIGA-340 Interface User's Guide* and the *TIGA-340 Interface Brochure*.

Call 1-800-336-5236, ext. 3526, or write Texas Instruments Incorporated, P.O. Box 809066, Dallas, Texas 75380-9066.

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AHE2815D	15	±15V, 0 - 500mA

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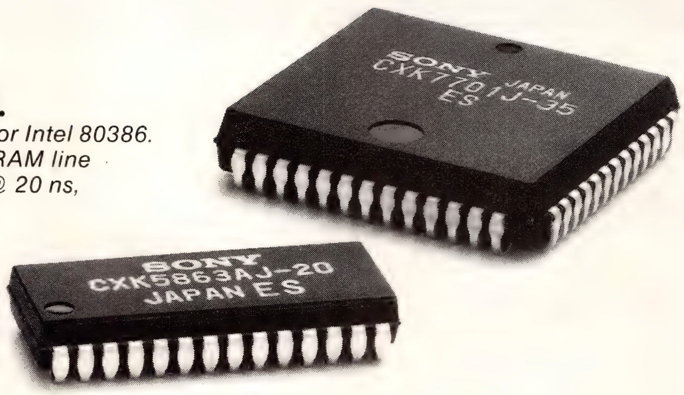
Cache memory for Intel 80386. Also standard SRAM line down to 8K x 8 @ 20 ns, 16K x 4 @ 15 ns.



What you see here is a demonstration of Sony's intense commitment to your each and every SRAM need.

A commitment made even more impressive by the fact Sony's only been engineering and producing SRAMs for just over five years.

And when you consider we're pouring all our resources into SRAM technology—including a new production facility in Nagasaki, Japan—this demonstration merely hints at the Sony SRAM technology yet to come.

Ultra-high speed cache.

Via a unique 0.8-micron process, Sony covers your fast processor cache-memory needs two distinct ways.

First, there's our Model CXK7701J, designed specifically for the Intel 80386.

This application-specific memory (ASM) combines address latch, memory and transceiver within one IC. Ready for user configuration as either an 8k x 16-bit memory or as two 4k x 16-bit memories.

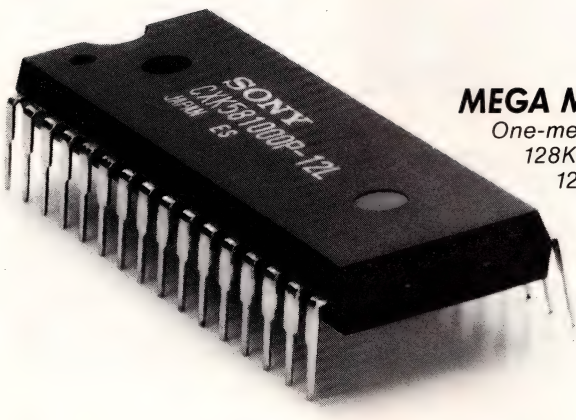
Second, consider our new ultra-high speed SRAM capabilities.

ULTRA-HIGH SPEED CACHE SRAMS			
MODEL	CONFIG.	SPEED (ns)	PACKAGE
CXK7701J*	8K x 16	30/35/45/55	PLCC
CXK5863AP	8K x 8	20/25/35	DIP 300 mil
CXK5863AJ	8K x 8	20/25/35	SOJ 300 mil
CXK5466P	16K x 4	15/20	DIP 300 mil
CXK5466J	16K x 4	15/20	SOJ 300 mil
CXK5467P**	16K x 4	15/20	DIP 300 mil
CXK5467J**	16K x 4	15/20	SOJ 300 mil

*For Intel 80386. **O/E

As you scan the chart above, keep in mind even higher speeds will be available soon.

S ITS SRAM
THE EXTREMES.



MEGA MEMORY.
One-meg SRAM line includes
128K x 8 @ 100/120/150 ns,
128K x 8 @ 70/85 ns,
128K x 8 @ 35/45/55 ns.

Ultra-high density.

Sony solves your board-space problems with three new 1-Mbit SRAMs.

Each is based on our 0.8-micron CMOS technology. Configured as 128K x 8 bits. And available in 32-pin DIP and surface-mount plastic packages.

And not only do Sony 1-Mbit SRAMs maximize board space, but process speeds as well.

Nowhere else will you find a greater choice: 100/120/150-ns, 70/85-ns and 35/45/55-ns speed figures.

HIGH-DENSITY SRAMS			
MODEL	CONFIG.	SPEED (ns)	PACKAGE
CXK581000P	128K x 8	100/120/150	DIP 600 mil
CXK581000M	128K x 8	100/120/150	SOP 525 mil
CXK581001P	128K x 8	70/85	DIP 600 mil
CXK581001M	128K x 8	70/85	SOP 525 mil
CXK581020SP	128K x 8	35/45/55	DIP 400 mil
CXK581020J	128K x 8	35/45/55	SOJ 400 mil

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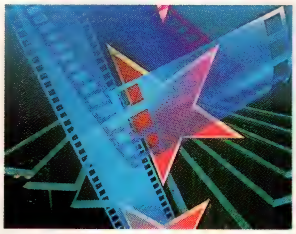
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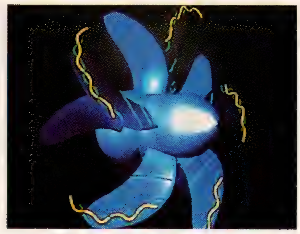
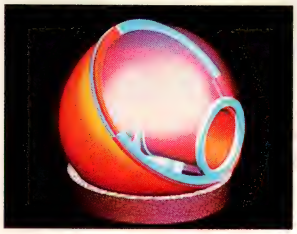

Computational fluid dynamics


Video animation productio


Video animation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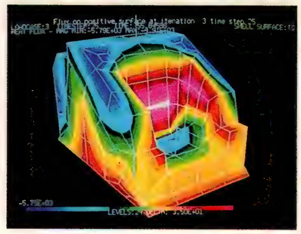
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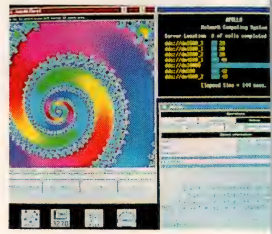
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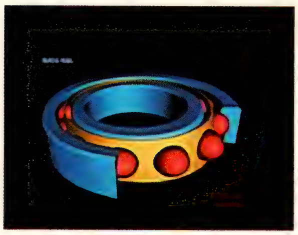
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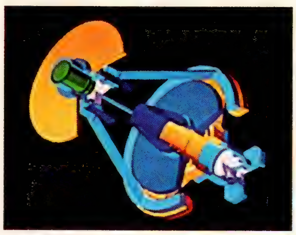
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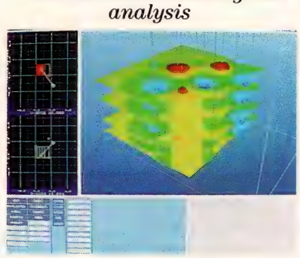
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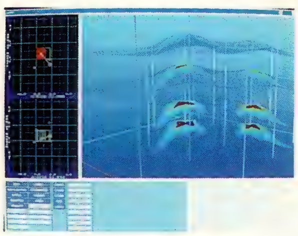
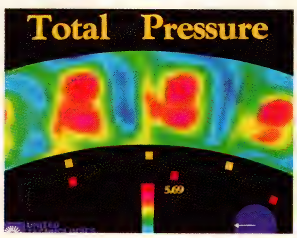

Reservoir analysis



Computational fluid dynamics


Industrial design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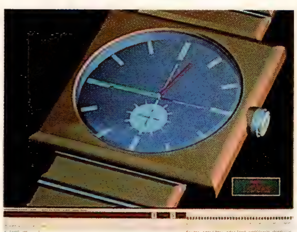
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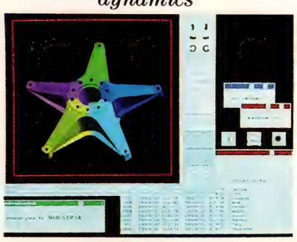
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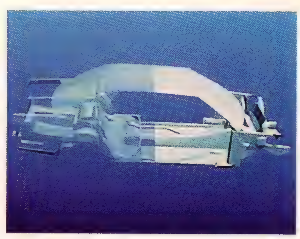
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Animation


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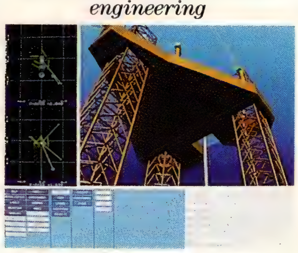
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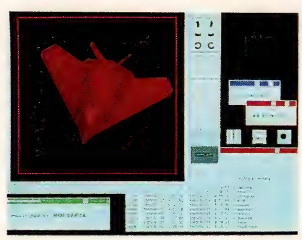
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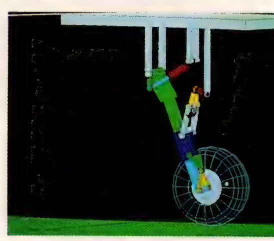
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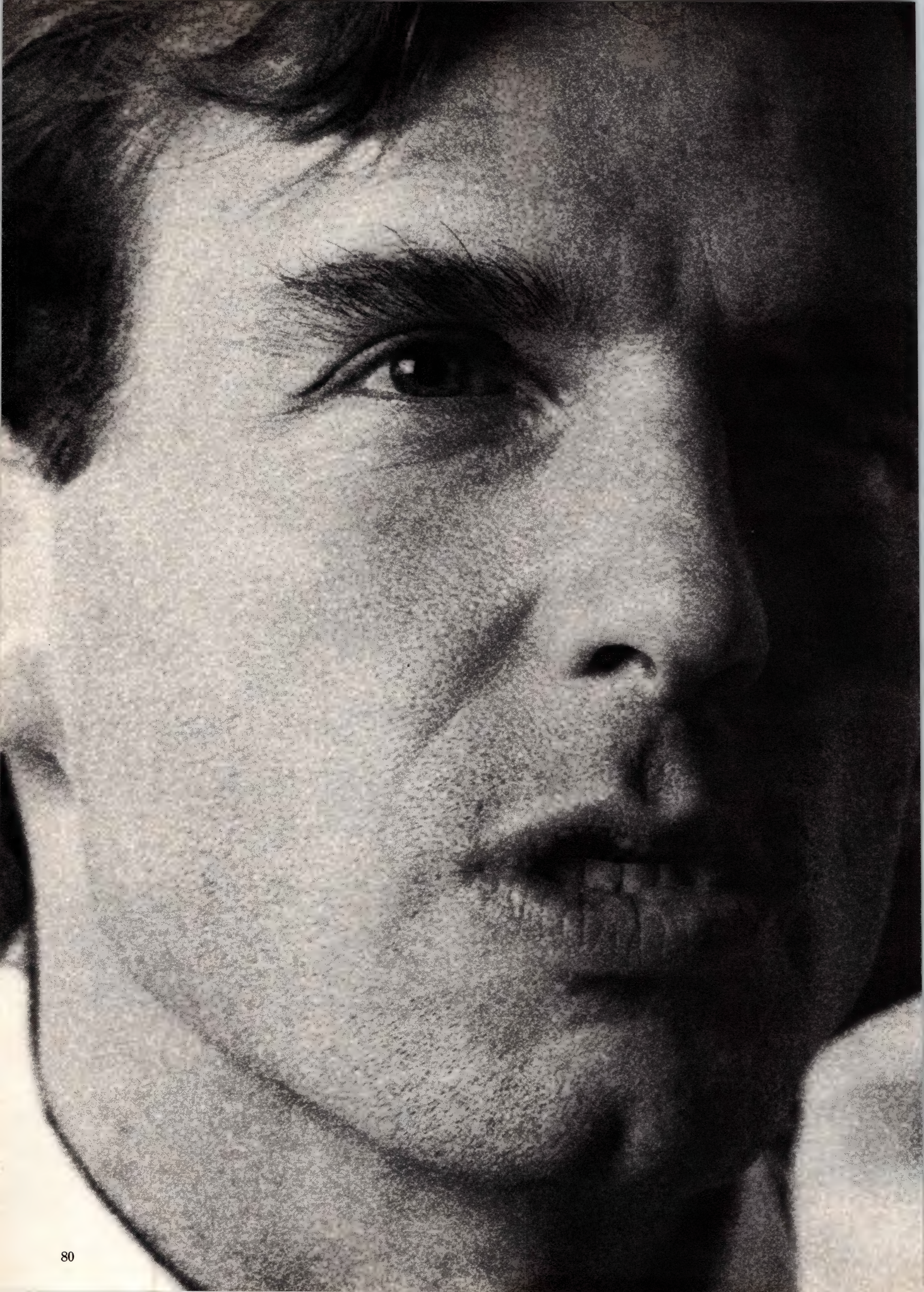

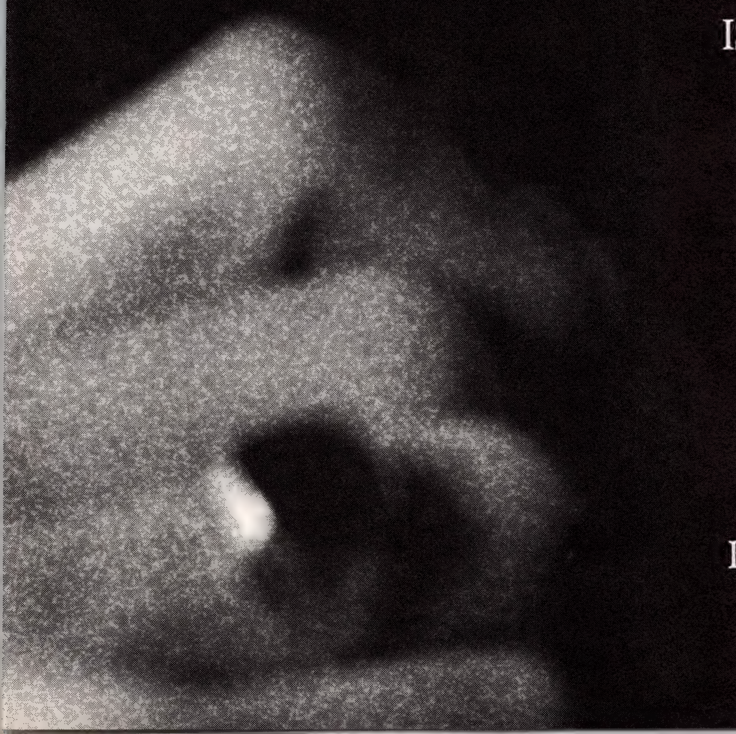

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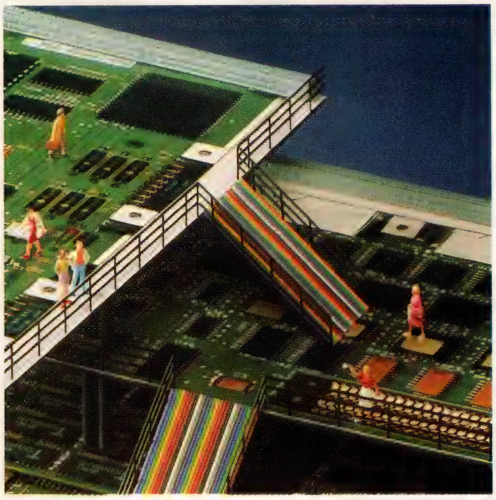


Add-on BUSES

Jon Titus, *Editor*

Add-on buses let you attach small I/O boards to your computer at low cost. However, these devices aren't without controversies, which revolve around technical issues, standards, and just how open the architectures of many add-on buses really are.

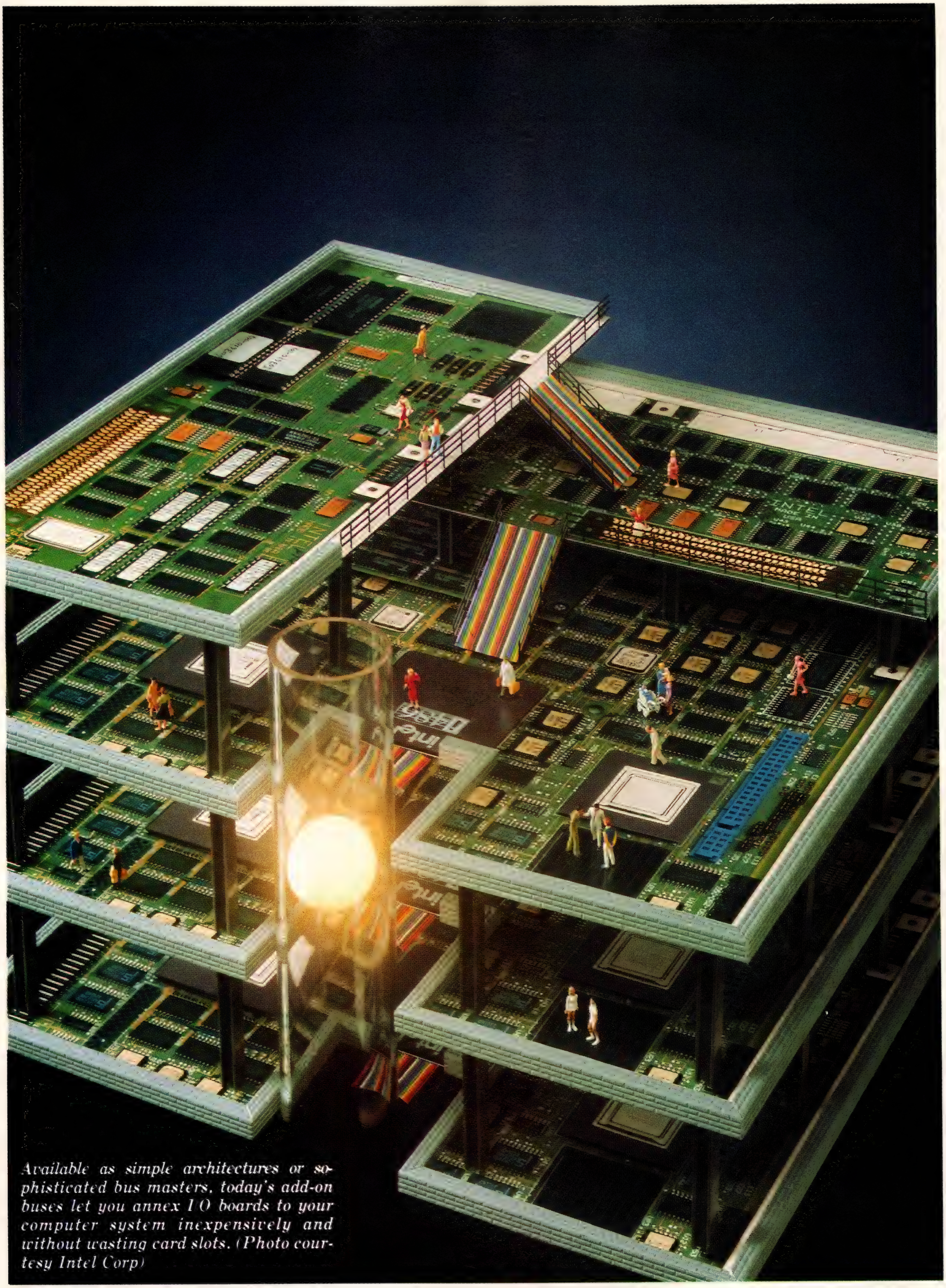
When you think of computer buses, VMEbus, Multibus, and the IBM PC/AT bus probably come to mind first. However, there are many other add-on buses that let you take a basic computer board and expand its use—usually at low cost. The popularity of these add-on buses stems from the need to add special functions to a computer system without occupying an extra slot or without adding expensive and special-purpose boards. Before you look at a specific bus, however, consider the ramifications of adopting a bus that may be supported—at least for now—by only one or two manufacturers.

In defense of add-on buses, Vic Serbe, an applications engineer at Central Data Corp, says that modular I/O connections and boards will always be popular. People want to plug in their boards, write their driver routines, and get the system up and running as quickly as possible, he says.

But not everyone thinks that the add-on boards are a panacea for I/O bottlenecks. Fred Rehhausser, director of strategic marketing at Force Computers (Campbell, CA), believes that gate arrays and ASICs can make board design easier. By adopting such VLSI chips, computer-board manufacturers have more room on their CPU boards for the functions that people need.

Laurent Meilleur, VMEbus product manager at Matrix, doesn't like add-on boards for simple devices such as A/D and D/A converters. He thinks that designers who need such functions should seek boards that connect right to the main bus and that offer those functions. "Overall," he says, "using add-on daughter boards can be more expensive than taking a single-board-computer approach. Some of those daughter boards are expensive!"

Another bus-related topic that comes up frequently is standards. Engineers often wish for standards that



Available as simple architectures or sophisticated bus masters, today's add-on buses let you annex I/O boards to your computer system inexpensively and without wasting card slots. (Photo courtesy Intel Corp)

Add-on buses offer great flexibility, but you must be willing to deal with only a few suppliers. Some manufacturers offer very few boards.

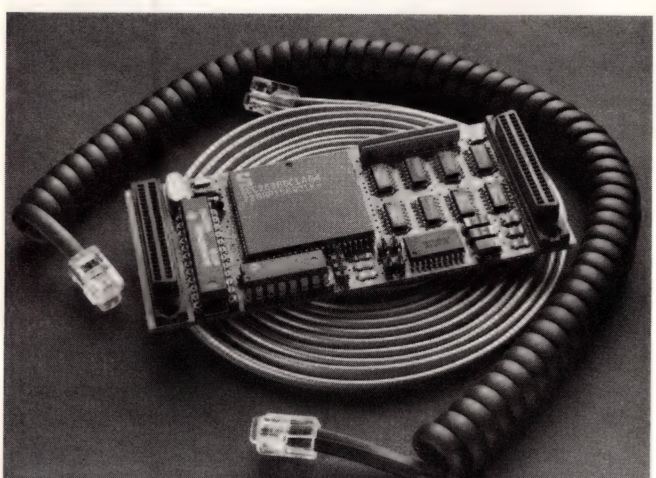
would unite the add-on-bus field behind only a few standard buses. However, the issue comes down to standard buses *vs* flexibility for designers. According to Rehhausser, "The add-on buses are an attempt by small companies to defeat standards and to lock in customers. Such manufacturers can get into the market by selling an inexpensive board and forcing customers to buy add-on boards later."

Markets set standards

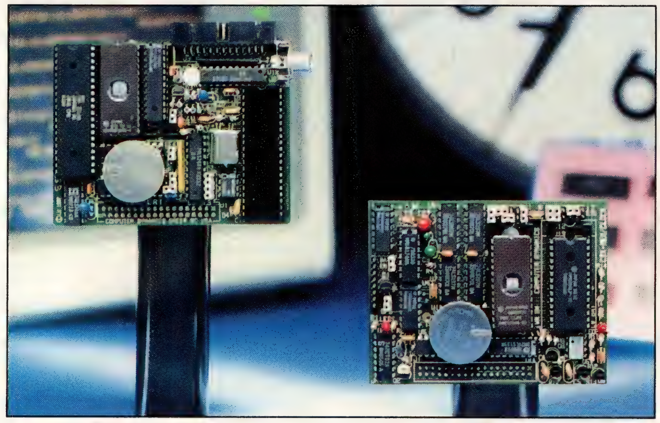
"In most cases, the market should set the standards. It's OK for standards to apply to the computer backplanes, but let's put our creativity into the add-on-bus products," says Del Miller, General Micro Systems' vice president of sales and marketing. He adds, "Anyway, why would anyone want to put a Brand-A add-on board onto a Brand-B CPU board? At the add-on-bus level, standards may be an answer to a question that no one is asking."

Kim Rubin of Greenspring puts standards in another light. "You may have a system that doesn't fit a standard—it's not a VMEbus-based system. Maybe it's one board running a piece of equipment, say an automated cash register. You shouldn't have to force someone to use a standard bus. Let them add one small board that customizes the unit to meet the customer's needs."

Rehhausser says that standard buses are available and that designers and users of VMEbus products should take a careful look at the VMEbus's existing VSB (VME Subsystem Bus), which expands a CPU board's capabilities. He says that communication



***Eight serial ports** are available on Greenspring Computers' IndustryPack add-on board. Two holes on each connector let you use machine screws to fasten the unit to a baseboard.*



***Typical SBX boards** are small, but they can still hold a lot of circuitry. The board on the left is a video controller, and the one on the right is a real-time clock that can accommodate as many as 128k bytes of memory. Because of the SBX bus's limited addressing capability, the clock chip sequences through memory addresses for block-transfer operations.*

boards now plug into the VSB and that SCSI-controller boards aren't far from market. Rehhausser stresses that the VSB is a standard now. In fact, Motorola, Radstone, and Ironics all offer VSB boards.

We'll assume that after considering the arguments above, you're still interested in learning more about add-on buses. To give you a better idea of what the add-on-bus world encompasses, we'll examine seven buses, from the simplest to the latest introduction. Our representative sample, including the products in **Table 1**, gives you an idea of what you have to choose from. In some cases, however, your choice may be limited to the products available from only one manufacturer.

Start with the SBX

Perhaps the earliest add-on bus arose from Intel's popular Multibus (now Multibus I, or IEEE-796) in the late seventies. Within the Multibus specification, the iSBX (Intel System Bus Extension, or just SBX bus, as it's popularly known), provides a way of adding small I/O boards to a main processor board, or baseboard. Many processor boards let you add as many as three SBX boards. If you need to add more SBX boards to a Multibus I system, the CD21/6600 SBX Motherboard ($710) from Central Data supplies six independent SBX connectors on one Multibus I card. (Unless noted otherwise, all prices are for unit quantity.)

In general, the SBX boards supply a variety of functions and interface circuits for serial communications

or for digital and analog I/O. Most SBX manufacturers supply interface circuits on single-wide boards that measure 2.85×3.70 in. Manufacturers may also supply double-wide SBX boards that measure 2.85×7.5 in. Typical of dual-wide SBX boards is the LSBX Serial/4 board ($325 (100)) from Computer Modules, which lets you control four serial I/O ports. Keep in mind, though, that the longer boards can hang over the sides of the main board depending upon which SBX connector you plug them into.

Often you have a choice of 8- or 16-bit SBX boards. The 8-bit boards will operate in 8- or 16-bit systems, but you can't adapt 16-bit SBX boards to operate with 8-bit computer boards. The Multibus specification allows two connectors—an 8-bit 36-pin connector and a 16-bit 44-pin connector. A 36-pin SBX-board connector can mate with a 44-pin connector on a baseboard.

Boards furnish inexpensive I/O

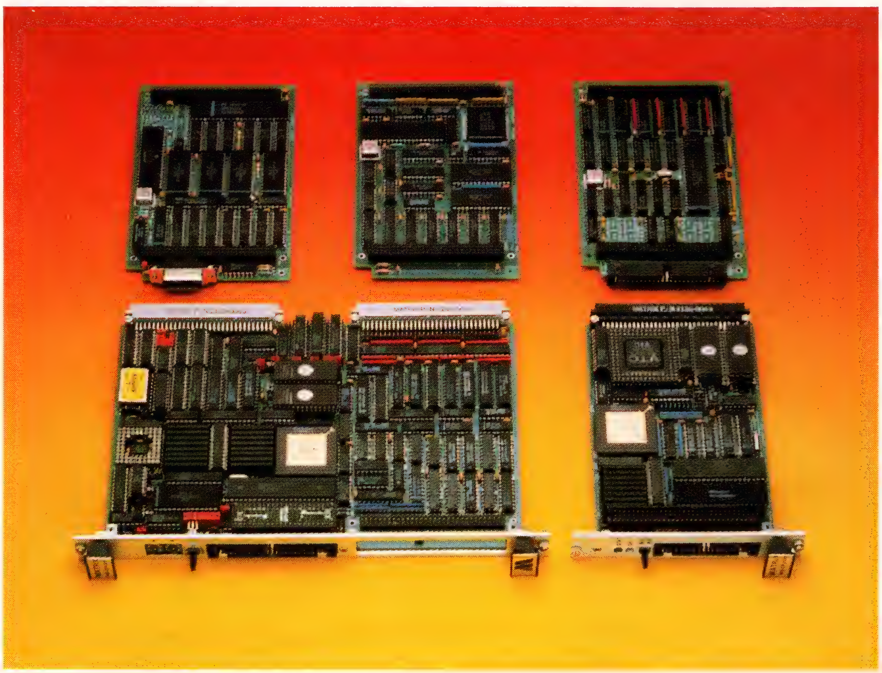
According to Vic Serbe at Central Data, the SBX is a success because it provides an inexpensive way to get I/O into your computer. However, Serbe cautions that some of the newer buses may avoid incorporating simple add-on buses such as the SBX. Because the SBX provides only a rudimentary bus for I/O devices, SBX boards can't provide much 'intelligence.' As a result, the add-on boards can actually decrease the performance of the system by wasting the CPU's time. For example, a serial I/O board typically requests service after it sends or receives each byte. In a VMEbus- or Multibus II-based computer, developers must avoid tying up the CPU with such trivial tasks.

SBX boards still have a healthy future. Although each SBX board offers only one or two functions, SBX boards remain popular, and the market is still growing as manufacturers upgrade and expand equipment that relies on Multibus I computers and boards.

Steve Cooper, director of marketing at Radix, notes that although many SBX boards rely on DMA operations to transfer data quickly to and from memory, not all of the baseboards support DMA operations. Thus, if you want to use an SBX board that requires DMA operations, check the baseboard's specs before you design.

Generally, SBX boards cost from more than $100 to more than $500. Typical examples of SBX boards include a counter-timer and parallel I/O board from Computer Dynamics (CDX-CTC/PIO, $300) and an SCSI interface board from Single Board Solutions (SBSx SCSI/CEN, $195).

In addition to working with Multibus I computers, the SBX offers a way to expand the STD Bus—a bus already known for a wide variety of low-cost I/O boards. One of Ziatech's 80188-based CPU boards for the STD Bus incorporates an SBX connector and interface. Phil Nash, Ziatech's marketing-communications



Boards for the Dbus-68 *fit on either a 6U VMEbus board (left) or a 3U VMEbus board (right). You can choose from a variety of peripheral-control and general-purpose I/O boards for the bus.*

Today's add-on buses range from simple I/O controllers to sophisticated master/slave control units, but don't buy more flexibility than you need.

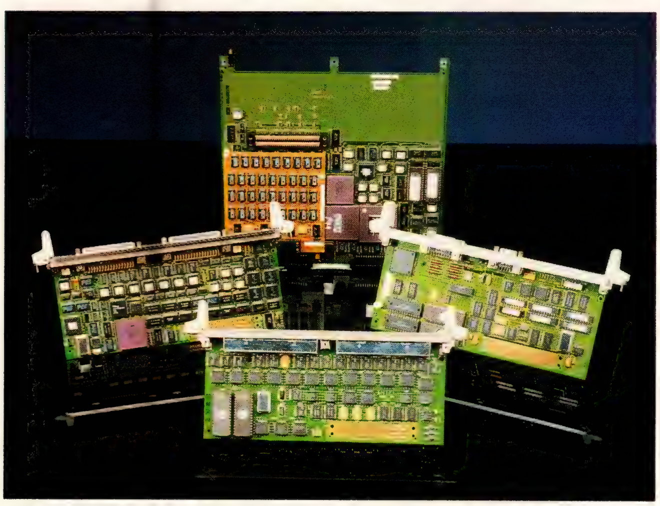
manager, says, "Even if the added height of the SBX board means leaving an open slot in the card cage, STD Bus slots are cheap." Nash says that Ziatech will continue to offer SBX connections on new products as the need arises, but they won't be offered on high-end products—on an 80386-based computer, for example.

If the idea of adapting SBX boards to the STD Bus appeals to you, you may want to consider Inovec's STD/SBX card ($210), which accepts two single-wide SBX boards and occupies one STD Bus slot. The company also supplies several SBX boards.

Kim Rubin, the vice president of engineering at Greenspring Computers, says that Greenspring considered using SBX boards, but the resulting assembly can't fit into one card slot when mated with a VMEbus or Multibus II card. "A wasted card slot in VMEbus or Multibus II systems costs you 5% of a 20-slot enclosure," says Rubin, and he cautions, "Not all SBX boards work in all SBX connectors."

Watch for undefined signals

Indeed, the SBX specification does show two undefined Option signals that users can connect for their own needs. The specification also describes two Reserved signals that may be defined in the future. The improper use of those signals can lead to confusion, but boards built to the defined signals should operate according to the IEEE-796 specification **(Ref 1)**. However, the specification (Rev 0.6) for Greenspring's IndustryPack boards also lists two Special Function pins that aren't well defined.



***Add-on boards for the MIX** attach to a Multibus II baseboard (rear). Each add-on board supplies its own front panel and pads for an SMT board-to-board connector. Connector pads are visible at the bottom right edge of the frontmost board.*

Nevertheless, Rubin claims that his company's interface design is independent of any specific bus or CPU. He backs that claim by pointing to the VIPC310 ($410), a VMEbus 3U carrier that holds two IndustryPack boards, and to the SupportBoard 1270 ($295), which puts two IndustryPack boards on the Apple Macintosh's NuBus. The company also sells a VMEbus 6U carrier that holds four IndustryPack boards. Typical IndustryPack boards range from $240 to $520 each. Most of the boards are single-wide units, but the carriers also accommodate dual-wide boards that take two single-wide positions.

Unlike some add-on buses, the IndustryPack architecture requires an onboard identification (ID) PROM that may hold as many as 64 16-bit words. The PROM contains a manufacturer ID number, details about the board, and perhaps I/O configuration data. Greenspring furnishes each manufacturer with a free ID number. The PROM helps the main computer system configure the I/O channels and devices. Rubin claims that by storing configuration data in the PROMs, the cards require no jumpers and no installation programs. The company also provides a complete memory map in its specifications booklet.

Some boards suit several μPs

In the add-on-bus field, the IndustryPack architecture isn't alone in claiming compatibility with many CPU boards. You can adapt Matrix Corp's Dbus-68 (or just Dbus) to other buses, too. However, as it's used by Matrix, the bus lets users add expansion boards to either 3U- or 6U-size VMEbus cards. When you add a Dbus board to a 3U-size card, the complete assembly requires two adjacent VMEbus slots. When you use a 6U-size card, however, the components on both cards face each other, and the assembly requires only one VMEbus slot. The signals and the connectors on the Dbus boards are exactly the same—only the add-on board's mounting position changes.

Besides picking up Dbus signals through a 64-pin connector, the Dbus boards also give you direct access to the signals on rows A and C of the VMEbus's P2 connector. These signal lines help you overcome another serious bottleneck: getting I/O signals to and from your computer boards. The P2 connector lets you route I/O lines out the back of the computer system instead of cluttering the front panel with connectors and cutouts for cables.

For example, Matrix offers a Dbus board that sup-

Consider bus selections carefully

Consider the following general guidelines before adopting an add-on bus for a system you're building.

Determine whether an add-on bus supports both master and slave devices. Slave devices are simple I/O circuits that transfer data to and from the computer and I/O devices. On the other hand, if you plan to connect intelligent devices to your add-on bus, you may want them to be able to take control of the bus to transfer information and commands to other devices without having another board intervene. If you need such bus-master capabilities, be sure that the add-on bus supports them.

Also, be sure that the widths of the data and address buses will meet your needs. For example, you can't use the three address lines on the SBX bus to address more than a few I/O locations. Likewise, you may not need all of the addressing capabilities of the Heurikon Corebus unless you plan to greatly expand the memory or use dual-port memories to control a peripheral processor.

Don't let power consumption become a last-minute consideration. A design without enough power or ground pins or insufficient current-carrying capacity at the connectors is an easy trap to fall into. If you're designing your own add-on board, do a power budget after you have a rough design to be sure you aren't facing a brown-out on your board.

Kim Rubin at Greenspring says that a good connector should protect the pins and contacts and that it should be impossible to mate connectors improperly. Be sure you ask how many insertions a connector's contacts can withstand. Greenspring claims that its connectors can withstand as many as 200 insertion cycles. About 100 insertion cycles is the limit for DIN connectors, and some cheap DIN connectors die after only 25 insertion cycles.

Check the mechanical configuration of the add-on cards you plan to use or design. First, be sure that your circuit will fit on an add-on board; next, be sure that the complete assembly will fit in the space available. Don't assume that an add-on card won't take up an adjacent card slot. Make careful measurements and check them. Also, be certain that the system has space for cables and connectors and that they are readily accessible.

Because add-on cards are part of the overall mechanical system, you should know how add-on boards mount to the baseboard. The connectors and the add-on boards should be mechanically stable. Greenspring's boards fasten to its baseboard with four machine screws. SBX boards usually fasten with one screw. Some users have been known to plug in an add-on board without any mechanical fasteners. Don't rely on the connector's grip to hold your board in place; Fred Rehhausser at Force Computers says that certain add-on boards have a tendency to work out of their sockets. He adds that some designers put the chips so close to other components that heat builds up, and the circuits become unreliable.

You must demand complete documentation, too. Even though a manufacturer claims that its bus is nonproprietary, or open, you've got to see a complete package of documentation to prove it. Without the proper documentation, a so-called open bus defaults to being proprietary. When you examine the documentation, be sure that you get complete timing diagrams and timing descriptions as well as complete signal descriptions and signal names. Rehhausser also cautions buyers of add-on boards that interoperability of add-on boards can be a problem: "There are good technical people at these companies, but unless you're dealing with a real standard, specs can change—so buyers must beware."

You should also get complete schematic diagrams for the products you buy and for test circuits if you plan to adopt the bus for a product of your own. If a bus-interface design uses PLAs, you must receive complete listings for the PLA circuit. Sample software routines—particularly for the more complex buses—are a must. Don't be shy about asking for such information. You'll have to pay a small amount for some of the bus information, just as you'd have to pay for copies of an IEEE standard.

Acknowledgment

Thanks go to Laurent Meilleur at Matrix, who suggested many of the points in this box.

If you look far enough, you can probably find an add-on board that meets your needs. Offerings range from a few digital I/O lines to SCSI controllers.

plies an interface to an Ethernet network. When you order one of the DB-ETH cards ($600), you specify whether you want Ethernet signals brought out to a front-panel connector or to the P2 connector.

Lack of space spurs bus innovation

The Sambus from General Micro Systems operates in a similar fashion to the Dbus. Del Miller, General Micro Systems' vice president of sales and marketing, says quite frankly that the company developed the Sambus because its main computer boards ran out of space for I/O functions. Therefore, the company's engineers extended all the CPU's pins to an expansion connector. According to Miller, "When you extend the CPU's signals, you get at all of the μP's capabilities."

Miller can't understand why engineers design special add-on buses when a CPU's signals are readily available. He says that some companies may have difficulty designing add-on boards for their own computers because one CPU-board architecture may not adapt to all the various I/O functions and μP chips.

To the designers at General Micro Systems, providing all of the CPU chip's signals on the Sambus meant that the add-on boards would work just as if they were included on the main CPU board. Thus, the Sambus lets you add memory or I/O boards to the main computer board. For example, you can expand the CPU's main memory with a GMS SRAM (static RAM) board ($2495) that furnishes 1M byte of 35-nsec CMOS SRAM. Similarly, the company's GMS 1553 board ($1295) lets you add an interface for MIL-STD-1553 applications.

Miller says that General Micro Systems keeps its CPU boards "lean and mean" so that users can add the capabilities they want as they need them. For example, he says that designers of multiprocessing systems don't necessarily want I/O circuits on each CPU board. But they gain an advantage by building their systems around the same make and model of the baseboard CPU cards, because users don't want to learn about the peculiarities of four or five different types of CPU boards.

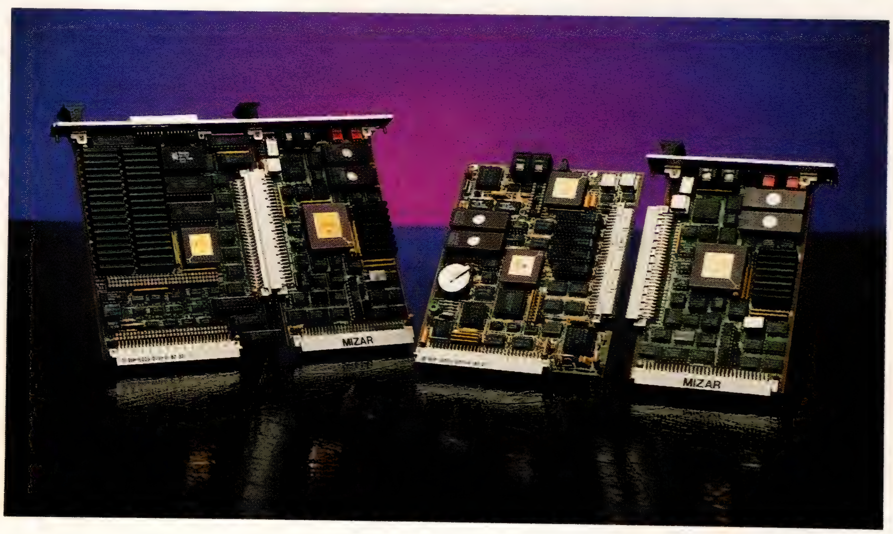
Add-on boards control VSB, too

Like the Dbus, the Sambus supplies a 64-pin connector near the P2 bus connector, which gives you access to the P2 connector's row-A and -C signals. The VMEbus's VSB (VME Subsystem Bus) signals aren't supplied on the General Micro Systems CPU board. However, if you need those signals, you can use a Sambus GMS VSB board ($495) to generate them and put them on the P2 connector.

The VMEbus has gained a large following, but the Multibus II hasn't yet gained widespread popularity. Therefore, it remains to be seen how many third-part OEMs will gravitate toward Intel's MIX (Modular Interface Extension) bus as a way of expanding the I/O capabilities of Multibus II-based computers.

Intel aims its MIX at designers who want a 32-bit bus for the I/O expansion of Multibus II boards. Introduced in the fall of 1989, the MIX includes a baseboard assembly that supplies power connections and mechanical support as well as the hardware, software, and firmware to link MIX boards to the Multibus II.

Because it supplies not only interface logic, but also bus-arbitration logic and shared memory, the MIX



***The MXbus converts 3U VMEbus boards** to 6U-size units as it expands the capabilities of the baseboard. Unlike most add-on boards that stack on top of one another, the MXbus adds cards to the side.*

Manufacturers of add-on buses and bus products

For more information on add-on buses and bus products such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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Performance Technologies Inc (I/O Pak)
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NOTE: Specific add-on buses are noted in parentheses after each manufacturer's name. Keep in mind that these manufacturers may also offer other types of bus products.

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High Interest 488 **Medium Interest** 489 **Low Interest** 490

Open buses may not be open if one company controls the standard. Before starting a design, get all the specs.

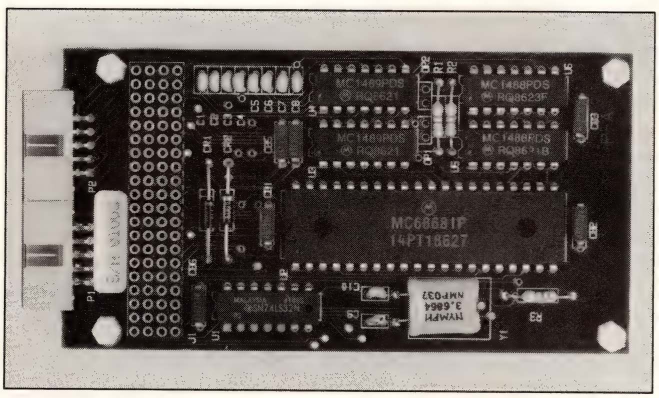
baseboard is the basis for a sophisticated add-on bus. Unlike most add-on boards, which act as slave units, a MIX add-on board may act as either a bus master or a slave. The baseboard assembly also furnishes firmware that controls the built-in self-test routines and the power-up configuration of the MIX boards. Intel offers MIX developers its MIX 386/020 baseboard unit ($2195), which comes with a 20-MHz 80386 μP and 1M byte of dynamic RAM (DRAM). You can also buy a complete MIX Module Development Kit for $4820. The development kit supplies the CPU baseboard, a test board, a breadboard, and a debug board. Intel also supplies a complete documentation package.

The MIX lets you stack as many as three boards on one baseboard. Unlike other buses that fit more circuitry into one card slot, the MIX requires one slot per board, and each board furnishes its own front panel. You can use the front panel's space for switches, indicators, and connectors.

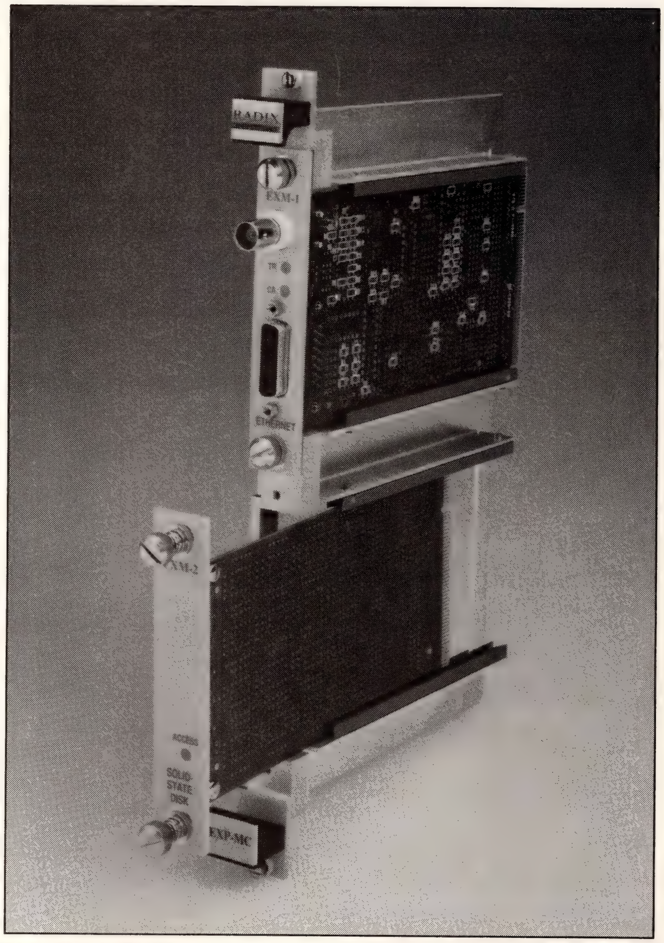
Paul Mesibov at Pentek is among the small group of designers who have designed and built MIX boards. He chose the MIX architecture so that he could concentrate on designing a high-speed data-acquisition system while buying computer boards from Intel. Mesibov says that it took him about three weeks to develop a working prototype from the MIX spec. He stresses that he built a slave board and that a bus master might take longer. The final product is Pentek's 12-bit, 10-MHz A/D converter board ($3995) for DSP applications.

Mesibov faced a significant problem with the MIX connector. Unlike almost all other add-on boards, which use plugs and sockets, the MIX boards require a surface-mount technology (SMT) connector. The connector sandwiches between the boards and makes contact with gold-plated pads on each board. The connector is a bit tricky to use; to mate it properly, you may have to add a Phillips torque screwdriver to your toolkit.

Mating the connectors isn't the toughest part of building a MIX board, however. Mesibov's design could have used a 2-sided pc board, but he had to design a multilayer pc board just to get the signals away from the SMT connector without electrical and mechanical problems. The connector also introduces a gold-plating problem. Your pc-board fabricator must be able to selectively plate gold over nickel on the 130 contact points for the connector. Unlike an edge connector, you can't run a plating bar between the contacts and cut it off at the end of the board-fabrication process. Mesibov



***You can add two RS-422 channels** to Omnibyte's VMEbus baseboard by connecting an Omnimodule OM/2SA4 board. The I/O connectors let you route cables through the baseboard's front panel.*



***You can get PC/AT-type cards** for VMEbus computers by using the EXM bus from Radix. The company redesigns PC/AT cards so that two of them fit into a 6U VMEbus slot. Radix supplies a '386-based CPU that controls the add-on cards.*

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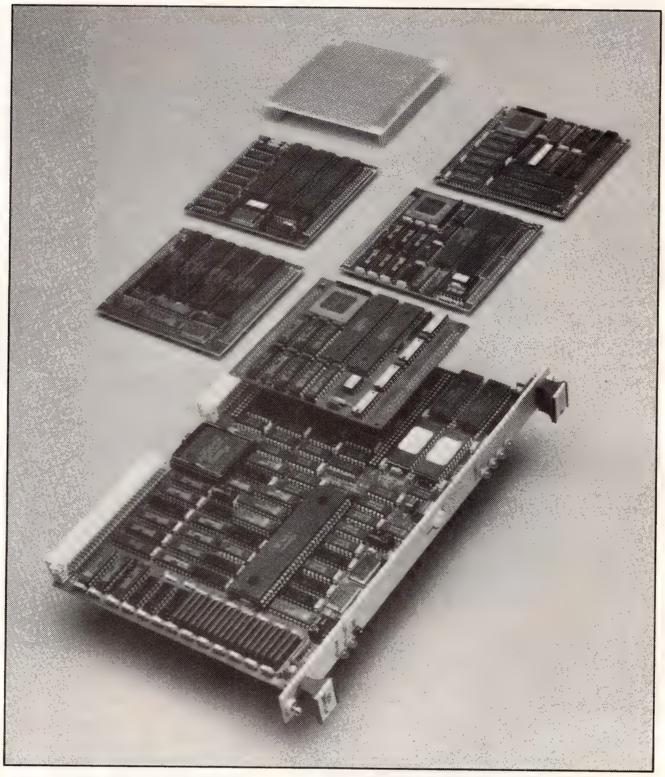
CIRCLE NO. 47

Several processor-independent buses lend themselves to original designs, so you can customize your product with existing add-on boards.

suggests that MIX-board designers be very picky about the pc-board fabricator they select. Also, he adds, be sure that you can fit your circuitry on a MIX add-on board that measures 3.45×7.79 in.

You can choose from several other buses that let you expand a basic computer system and in which the added boards are designed to occupy card slots. Like the MIX, the cCBX (Concurrent Technologies Bus Extension) from Concurrent Technologies expands Multibus II computers. However, instead of stacking add-on boards on a carrier board, the cCBX uses the Multibus II's P2 connector.

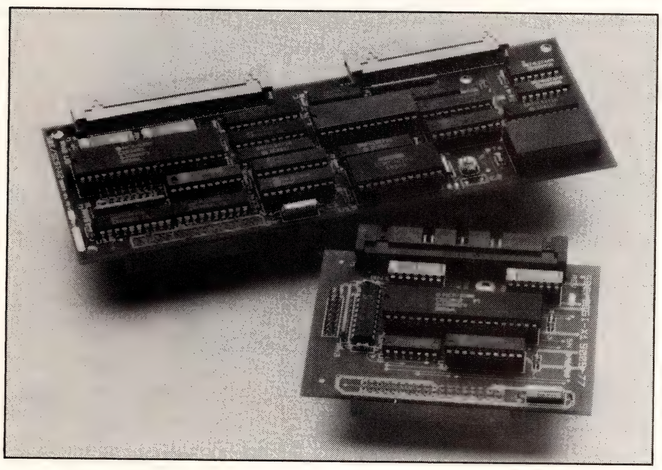
Glen Fawcett, the president of Concurrent Technologies, says that the US Government agencies he deals with favor the Multibus II architecture. Unfortunately, few Multibus II-compatible I/O boards are manufactured. "We designed a basic 80386 CPU board and developed slave boards for it—typically for DSP applications. Our cCBX interface signals go out the P2 connector to our other boards," says Fawcett. The company's basic Multibus II, CPU/cCBX-interface board furnishes an 80386 chip (16 MHz) and as much as 1M byte of memory. Prices start at $3950.



The I/O Pak cards access the VMEbus's P2 connector. *The add-on boards also offer a variety of functions that you add to Performance Technologies' basic CPU board.*

The cCBX controls four slaves

Bus-timing and bus-termination characteristics limit you to one CPU and to as many as four slave boards on the cCBX bus. However, your system can incorporate other Multibus II boards that communicate with the Concurrent Technologies CPU board over the main Multibus II Processor System Bus (PSB). Concurrent Technologies sells four types of slave I/O boards for cCBX systems. Complete specifications for the cCBX are available from the manufacturer.



Two sizes of SBX boards *let manufacturers put more circuits on one card. These two modules from SBE are SCSI-bus controllers. The smaller board supplies one SCSI port, and the larger one offers two SCSI connectors.*

Software isn't a big issue for Fawcett. He says that the cCBX is "nonexistent" to users because their software treats cCBX boards as system resources—it doesn't know that a cCBX bus is there.

Prior to deciding on the cCBX architecture, Concurrent Technologies also examined the IBM PC/AT bus as a candidate for its add-on-bus efforts. But Fawcett says that it wasn't obvious how to put the PC/AT bus into the Multibus II interconnect space. (Both Intel and Siemens/Micro Industries offer PC/AT add-on buses for the Multibus II architecture. Intel calls its extension P2/aPC, and Siemens labels its extension AT96, but these buses are beyond the scope of this article.)

However, Radix Microsystems pursued the PC/AT bus and adapted it to the VMEbus. Instead of developing a conversion scheme that fits existing PC/AT boards into a VMEbus-type enclosure, Radix redesigned PC/AT cards to a 3×6-in. size so that two of

Real products for real people.

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Several manufacturers give you access to the P2 lines on the VSB. This access is vital if you plan to use VSB add-on cards.

them would fit—one over the other—into a 6U VMEbus slot. The boards don't plug into the VMEbus; instead, they plug into a subplane board that fits on top of the normal VMEbus connectors. In turn, that subplane board mates with the company's EPC-3P CPU board, an 80386SX-based computer board that costs $2595 (100). The CPU board also connects to the VMEbus so that it can communicate with other VMEbus boards. The individual PC/AT-like boards are called Embedded-PC Expansion Modules, or EXMs.

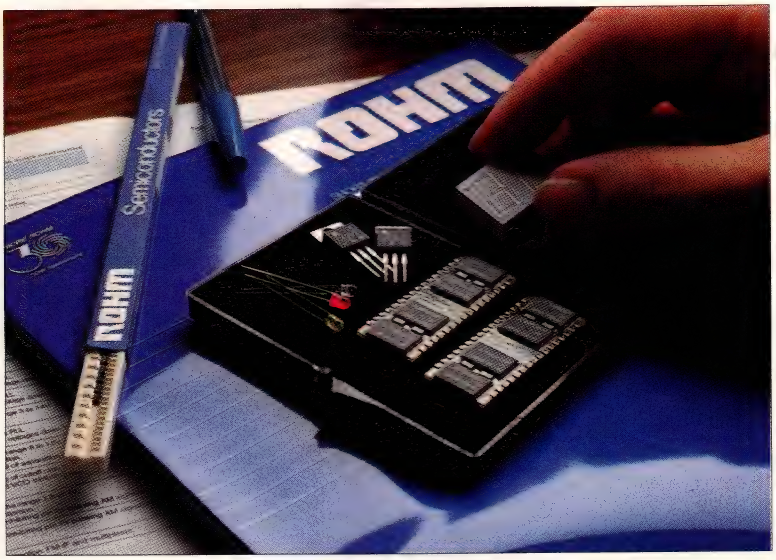
You may wonder why anyone would want a PC/AT computer as part of a VMEbus-based computer system. According to Steve Cooper, director of marketing at Radix, many people building VMEbus-based computers want the PC for its I/O functions. Those designers, asserts Cooper, don't want to go out onto the

Table 1—Representative open add-on bus architectures

Manufacturer	Add-on bus	Main bus	Data bits	Address bits	Interrupts	License	Comments
Concurrent Technologies	cCBX	MB II	8 or 16	24	8	No	Intended for general-purpose I/O. Bus originates from P2 on the cCBX CPU board.
General Micro Systems	Sambus	VMEbus	32	32	1	No	Dynamic bus sizing. Includes 16,000 I/O addresses. Engineering and manufacturing support, sample software, PLA equations available free.
Gespac	MLX	G-64	8	4	1	No	Intended for general-purpose I/O. Software tools and routines are available free from Gespac.
Greenspring	IndustryPack	VMEbus	16 or 32	22	2 levels	Yes	ID PROM sets up configuration information. Design tools from the manufacturer cost from $15 to $545. Includes 64 I/O addresses.
Heurikon	Corebus	VMEbus	64	32	4	Yes	Intended for high-speed memory, general-purpose I/O, and auxiliary processors. Plug-in modules can control baseboard. Two separate buses for I/O and memory devices. Software drivers are available. Source code is available for $2500. License fee required.
IEEE	SBX	MB I and II	8 or 16	3	2	No	Now covered by IEEE-796 standard. Contact Institute of Electrical and Electronic Engineers (New York, NY).
Intel	MIX	MB II	8, 16, or 32	32	2	No	Intended for general-purpose I/O, and auxiliary processors—not for memory expansion or smart I/O cards. Software tools are available from $630 (debugger). Includes 4096 I/O addresses.
Matrix	Dbus-68	VMEbus	32	32	2	No	Intended for general-purpose I/O, communications, disks, analog and digital I/O. Dynamic bus sizing. Requires no special software tools.
Mizar	MX	VMEbus	16 or 32	23 to 32	see comments	Yes	Controls as many interrupts as the CPU chip makes available. Based on 680X0 µP chips, so users require standard 680X0 software-development tools.
Omnibyte	Omnimodule	VMEbus	16	8 to 12	2	No	Intended for general-purpose I/O. Not recommended for memory extensions or high-speed communications such as Ethernet. Software drivers and debugging software available from manufacturer.
Performance Technologies	E Pak	VMEbus	32	32	2	No	Intended for disk, communications, and general-purpose I/O. Designer's manual and prototype E Pak available for $200.
	I/O Pak	VMEbus	16	24	2	No	Intended for disk, communications, and general-purpose I/O. Designer's manual available for $200.
Radix	EXM	VMEbus	8 or 16	24	10	No	Subplane connector lets the baseboard control IBM PC/AT-type cards that supply I/O circuits. Uses standard PC/AT signals. Can access other VMEbus cards over the main system bus.
Siemens/Micro Industries	OME	MB II	32	26	4	No	Intended for general-purpose I/O. Only one master can exist on the bus. Communications between modules occur via multiport memory and mailboxes, registers, and FIFO memories. Manufacturer supplies tools.
Sun	SBus	None	8, 16, or 32	28	1	No	Intended for general-purpose I/O. Bus supplies 32 virtual address lines and one of seven shared interrupts. Development kit is available for $300.

Key:
cCBX = Concurrent Technologies Bus Expansion
EXM = Embedded PC Expansion Module
MB I = Multibus I
MB II = Multibus II
MIX = Modular Interface Extension
MLX = Micro Local Extension
MX Bus = Mizar Expansion Bus
OME = Onboard Module Expansion
Sambus = Special Application Module Bus
SBX = System Bus Extension

Real help.



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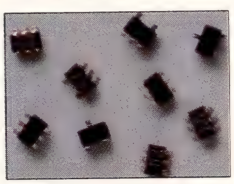

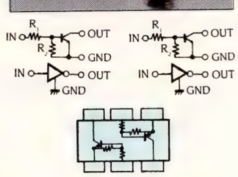

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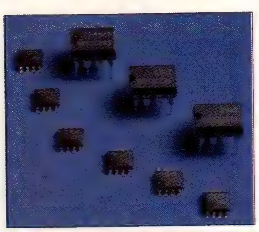
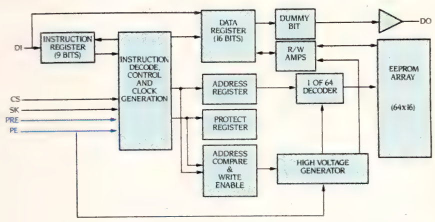


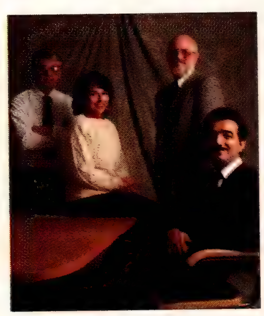
In addition to all the standard features you'd expect, the BR93CS46 operates at a low 2.7 volts, drawing only 20 μA. And you can even run it at a full 1 MHz.

The BR93CS46 gives you external read/write memory in sixty-four 16-bit registers, and interfaces with standard microprocessors like Intel's 8048/49/51/96, National's COP4XX, Motorola's 6801/05, TI's TMS1000, and Zilog's Z8. Seven 9-bit instructions control everything.



For more details, call Warren Schoals, the studious guy standing in the back. (Warren's also known as Mr. Whiteshirt when he's not out in his pick-up.)

Next time you're trying to figure out a solution that works today–or tonight–FAX us an S.O.S. Thank-you.



Then turn off the light and go home. Your family will thank you, too.

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CIRCLE NO. 49

If your application demands standard graphics and I/O, then consider adding a PC/AT to your system. At least one manufacturer puts a PC in VMEbus computers.

VMEbus for disk I/O and for network communications. Instead, they'd rather use peripherals already available for the PC/AT bus. The EXM bus's electrical specifications match those for the PC/AT, says Cooper, so people who develop EXM boards can use the PC/AT-bus information that has been available for some time.

Graphics capabilities are another boost for the embedded PC. "In the industrial market," says Cooper, "there are no graphics standards. On the other hand, the PC display has well-defined standards that most designers can use quickly. Also, people can start with a software standard such as Windows rather than worrying about bashing the display bits."

A VMEbus PC uses standard software

The PC on the VMEbus appeals to people who want to plug in the boards and have the computer up and running quickly. Cooper stresses that the PC cards come with ready-to-go software. Network boards are already configured and are ready to use with Netware or other standard software packages. The company now offers several EXM units—for example, an Ethernet/Cheapernet Controller (EXM-1), which costs $380 (100). You can also purchase a solid-state disk with either 1M or 2M bytes of flash EEPROM (from $590 (100)) and a SCSI and floppy-disk controller board (EXM-3). The disk controller costs $260 (100).

Workstation vendors are also finding the benefits of providing expansion or add-on buses. Sun Microsystems looked at many buses as candidates for expansion of the company's Sparcstation-1 workstation, but few of the available buses took advantage of today's advanced LSI chips and pc-board technology.

Workstations want buses, too

The Sbus grew out of Sun's search, and the new bus has drawn the interest of 200 companies that represent system vendors, hardware suppliers, and OEMs. Sun's SBus product manager, Steve Furney-Howe, says that 25 third-party suppliers are now working on SBus-based projects. Another indication of interest in the SBus is that LSI Logic Corp (Milpitas, CA) now offers samples of its L64853 DMA-controller chip ($76 (100)) for the SBus. Also, Sun isn't limiting itself to supporting the SBus on the Sparcstation-1 alone. The company will supply the bus in most of its new products.

Furney-Howe sees software as an important issue in the add-on-bus realm. To him, software drivers are part of the package that hardware manufacturers must deliver to their customers. Sun expects to support loadable device-driver routines for products that incorporate the SBus so that users don't have to completely reconfigure their systems as they connect add-on boards. Furney-Howe expects that most third-party vendors will write their own device-driver routines, but Sun also has a consulting group that can write drivers.

Sun now offers a 134-page manual of specifications for the SBus, and the booklet is free to interested developers. The company will soon ship its development kit, which will supply device-driver software as well as slave-device interface examples. Sun's SBus Support Group will also offer simulation models, firmware-development tools, and technical seminars.

The seven add-on buses we've discussed here should give you a good idea of the diversity of buses that can answer designers' needs for special add-on devices and circuits. It's impossible to cover all the add-on buses that people have designed over the last few years. For example, many bus adapters change one bus to another, and many adapters let you put one type of card into another bus system. Likewise, you can buy bus extensions that help a bus extend its life by expanding data- and address-bus widths. Look for articles on those units in future issues of EDN. EDN

References

1. Johnson, J B, and S Kassel, *The Multibus Design Guidebook*, McGraw-Hill, New York, NY, 1984.

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WHAT'S COMING IN EDN

EDN Magazine's February 15, 1990, issue will feature a staff-written Special Report on the role of static RAMs in systems with processing speeds exceeding 30 MHz. Part 1 of the designer's guide to Spice-compatible op-amp macromodels will describe a new approach to improving simulation accuracy. And EDN's occasional series about engineering in Europe continues with a report on the UK's Marconi Instruments.

Remember to look for our regular departments, too.


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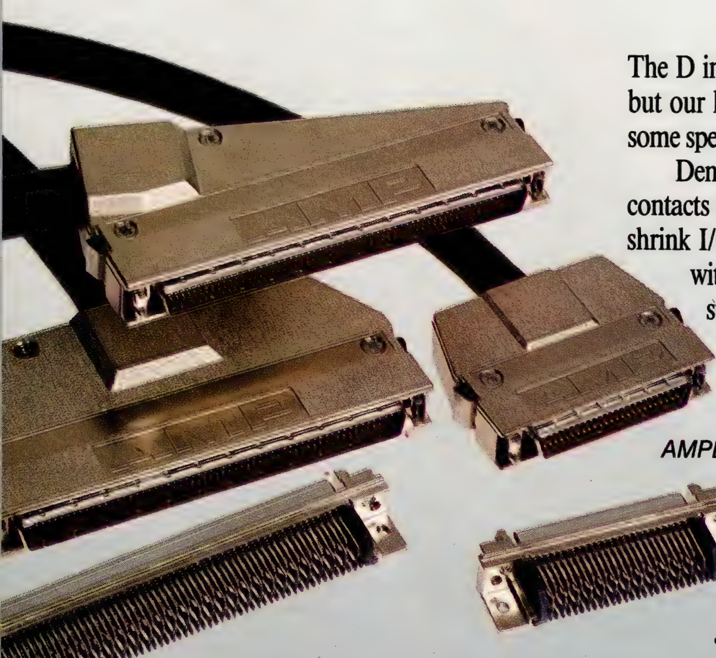

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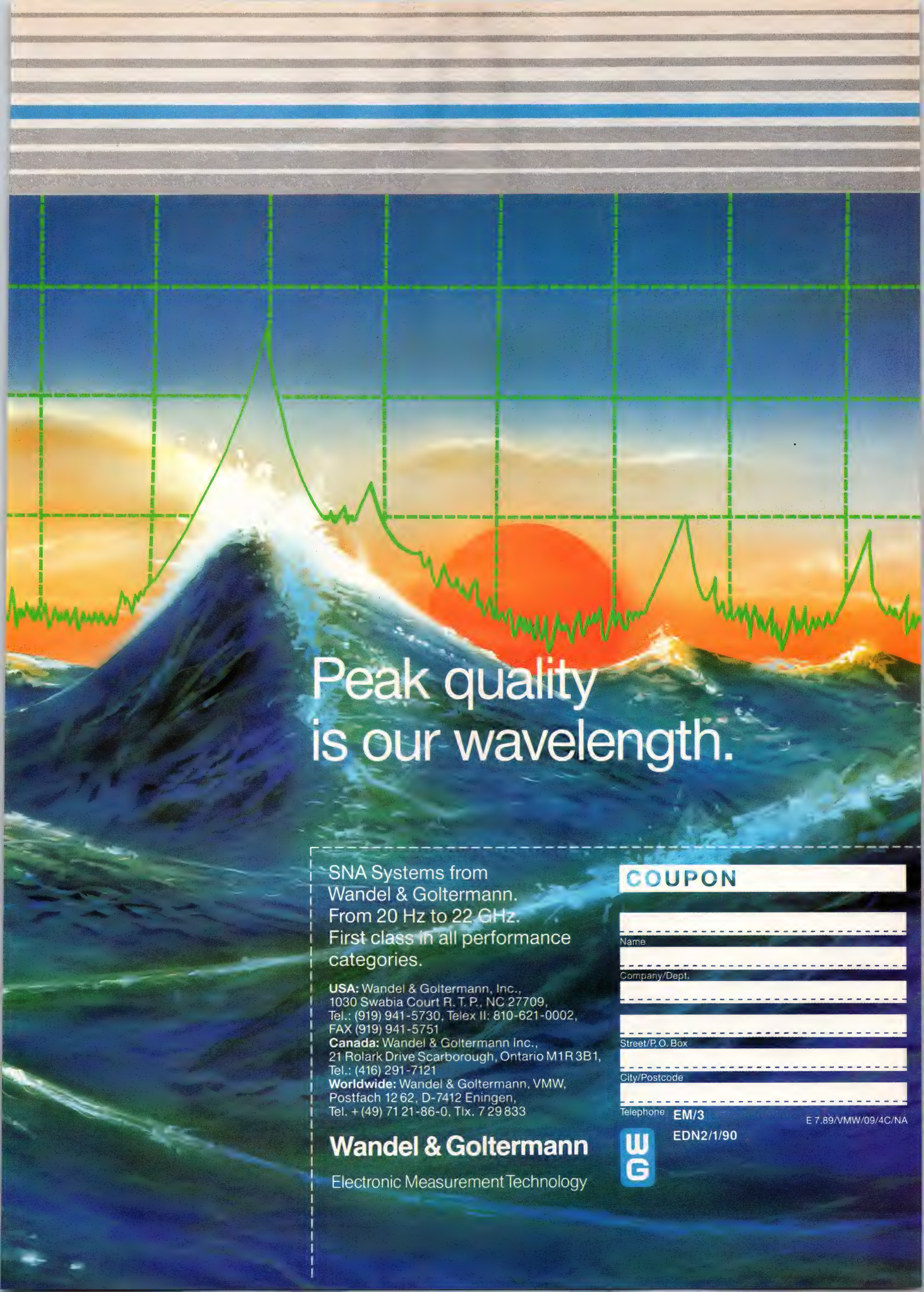
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DESIGNER'S GUIDE

flash–ADC testing
Part 3

Measure flash-ADC performance for trouble-free operation

The first two parts of this series described the subtleties of flash A/D converters and the test methods used to evaluate these devices. Part 3 concludes the series with a discussion of the actual measurements you'll need to fully characterize flash A/D converters.

Walt Kester, *Analog Devices*

Although manufacturers have expanded the number of guaranteed specifications they put on their data sheets, the test conditions often won't match those of your system design. You can use the methods described in Part 2 of this series to test a flash A/D converter, but the measurements you need to perform depend on the converter's primary application. This final part of the series provides information on important measurements you'll need to characterize your converter's performance, including total harmonic distortion (THD), differential and integral nonlinearity, and noise power ratio. You'll probably want to start with the S/N ratio, a measurement that's common to most A/D converter applications.

The S/N ratio is the ratio of the rms fundamental to the rms quantization noise. As described in Part 2, you can measure this parameter by digitizing a pure sine wave and performing Fourier transformations on the data. The rms energy contained in the fundamental sine wave is equal to the square root of the sum of the squares of the peak value and the values of the appropriate number of samples, or bins, located on either side of the peak. The converter's resolution and its side-lobe roll-off characteristics determine the number of samples you'll need. For a detailed explanation of sampling requirements, see Part 2.

The rms energy in the remaining frequency bins represents the noise due to theoretical quantization, the converter's harmonic distortion and excess noise, and the FFT round-off error. Take the square root of the sum of the squares of the remaining samples (excluding the dc components) to determine the rms energy. The overall S/N ratio of the A/D converter is

$$\text{S/N ratio} = 20 \log(\text{rms signal level/rms noise level}).$$

You can measure harmonic distortion in a similar manner. The test program (described in Part 2) examines the FFT frequency spectrum for the proper location of the desired harmonic (harmonics above $f_S/2$ will be aliased into the baseband) and determines the rms energy in that harmonic. The following equation calculates the harmonic distortion:

$$\text{Harmonic distortion} = 20 \log(\text{rms signal level/rms harmonic level}).$$

The S/N ratio and harmonic distortion are key specifications in evaluating the performance of A/D converters.

The total harmonic distortion (THD) is the root-sum-square of the first five harmonics of the fundamental. Use this number in place of the rms harmonic level in the above formula.

Two-tone intermodulation tests using FFTs

In many applications, you don't have the simple case of a single input frequency. For example, in communication applications that multiplex several frequencies onto a single carrier, you need to measure intermodulation products. You determine this parameter by applying two sine waves of different frequencies (f_1 and f_2) to an A/D converter. You then measure the amplitudes of the third-order intermodulation products, which occur at frequencies $2f_1+f_2$, $2f_1-f_2$, $2f_2+f_1$, and $2f_2-f_1$.

Although it's possible to filter out most intermodulation distortion if the two tones are of similar frequencies, the third-order products will be very close to the fundamental frequencies and thus difficult to remove.

To avoid clipping-induced distortion, the amplitudes of the individual tones should be at least 6 dB below the full-scale range of the flash converter. In addition, the frequency separation of the two tones should be consistent with the resolution of the FFT. As discussed in Part 2, the spectral resolution of the FFT is a function of record length M, coherence vs noncoherence, and the properties of the windowing function that you choose.

In receiver applications, you often want to know the maximum ratio between the amplitude of a single-tone input signal and the amplitude of its maximum spurious component. For an ideal A/D converter, this ratio occurs for a full-scale input sinusoid. In a practical A/D converter, however, spurious content is a function of slew rate. Therefore, the maximum spurious-free dynamic range for a given input frequency will probably occur at a level somewhat below full scale. Because the spurious-free dynamic range is slew-rate dependent, it's a function of input frequency and amplitude.

Fig 1 is a plot of the typical maximum spurious level vs input signal level. Also shown is a plot of the corresponding spurious-free dynamic range. The plot demonstrates that the maximum spurious-free dynamic range of 38 dB occurs for an input signal that's about 3 dB below full scale.

The data you need to generate these plots is readily available from the family of FFTs calculated for the different input amplitudes. By knowing the input signal level that gives the highest spurious-free dynamic range at frequencies close to the Nyquist frequency, it's possible to set the gain of the system to take maximum advantage of the A/D converter's spectral characteristics.

Histograms are helpful

Differential and integral nonlinearity are also important measurements of converter performance. Try a histogram test to obtain these measurements. To make a histogram analysis, digitize a known periodic input at a rate that's asynchronous relative to the input signal. To gather the sample data for the histogram, you'll need a buffer memory and a test system, as described

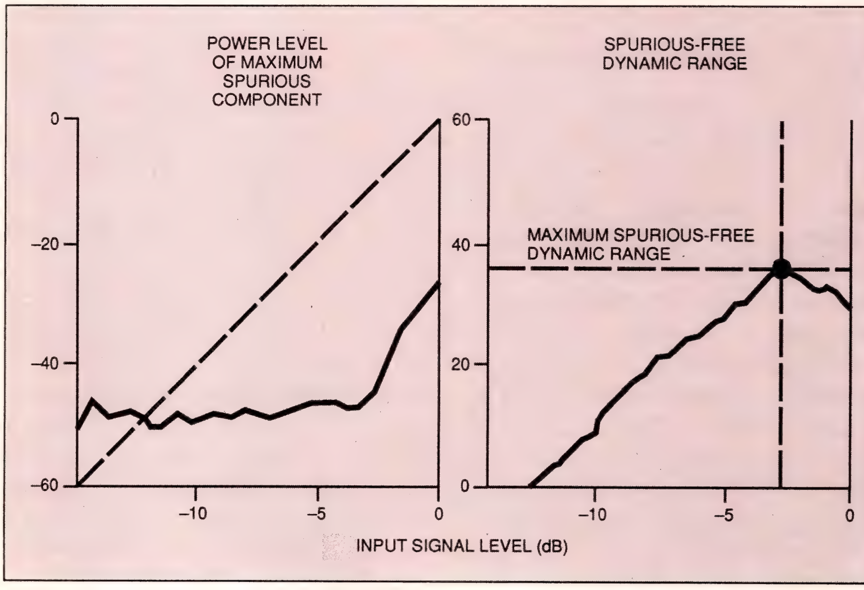


***Fig 1—These dynamic-range plots** show the power levels of spurious frequencies and the maximum spurious-free dynamic range. In this example, the maximum spurious-free dynamic range occurs at an input signal level that's 3 dB below full scale.*

in Part 2. The buffer memory will probably be too small to hold a statistically significant number of samples from a single run (several hundred thousand are usually required). For this reason, run several tests to acquire the data and load the contents of the buffer into the main memory of your test system after each run. Benchtop test systems from Hewlett Packard and Tektronix also provide histogram test capability.

After the test system accumulates a statistically significant number of samples, it can determine the relative number of occurrences of each digital code (the code density). This test routine then normalizes the data based upon the input signal and analyzes the results for linearity errors.

For an ideal A/D converter with a full-scale triangular-wave input, you'd expect an equal number of codes in each bin. The number of counts in the nth bin, H(n), divided by the total number of samples taken, M, is the bin width as a fraction of full scale. The ratio of the actual bin width to the ideal bin width, P(n), is the differential linearity. Ideally, this ratio should be unity. Subtracting 1 LSB gives you the differential nonlinearity.

You can determine integral nonlinearity with a cumulative histogram; the cumulative bin widths are the transition levels. However, the cumulative effects of errors can make the integral-nonlinearity measurement inaccurate. Histograms are used more often in evaluating differential nonlinearity.

High-speed, high-accuracy triangular waves are difficult to generate, so use a sine wave. All codes aren't equally probable with a sine-wave input, however, and you should normalize the histogram data using the probability density function for a sine wave, as shown in **Fig 2**.

To obtain accurate results, you need to take a large number of samples. For example, to determine the differential nonlinearity for an 8-bit flash converter to within 0.1 bit with 99-percent confidence, you'll need 268,000 samples. You can use hardware to count these samples, thus speeding up the software processing time. For high-speed sampling, decimate the output data to clock rates that are compatible with a slower-speed memory.

Using noise-power-ratio tests

You can use noise-power-ratio (NPR) tests to measure the transmission characteristics of frequency-division-multiplexed (FDM) communications links. In a typical FDM system, 4-kHz-wide voice channels are "stacked" in frequency for transmission over coaxial, microwave, or satellite equipment. At the receiving end, the FDM equipment demultiplexes the data and returns it to individual, 4-kHz baseband channels. In an FDM system that has 100 channels or more, Gaussian noise with the appropriate bandwidth approximates the FDM signal.

The test setup of **Fig 3** measures an individual 4-kHz channel for quietness by using a narrow-band notch (bandstop) filter and a tuned receiver **(Ref 4)**, both of which measure the noise power inside this 4-kHz notch. The NPR measurements are straightforward. With the

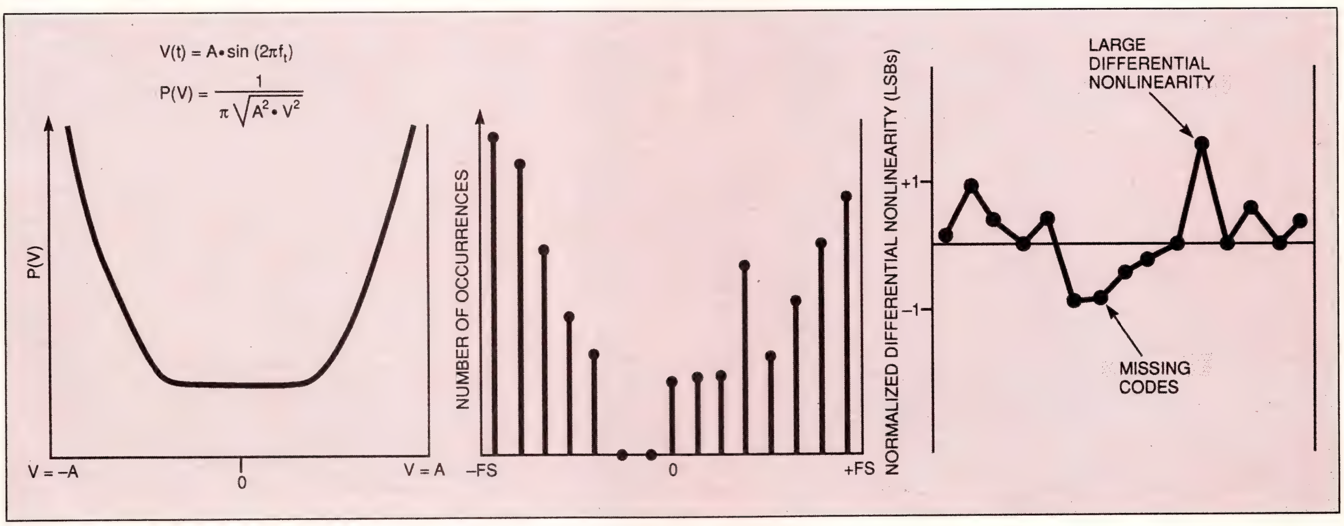


Fig 2—Histograms are often used to plot differential nonlinearity. *Shown here is a curve for the probability density function of a sine wave, which is used to normalize histogram data to produce a plot of differential nonlinearity.*

Where multiple frequencies exist on a single carrier, you need to measure intermodulation distortion as well as harmonic distortion.

notch filter out, the receiver determines the rms noise power of the signal inside the notch. The notch filter is then switched in, and the receiver determines the residual noise inside the 4-kHz slot. The ratio of the two readings, expressed in dB, is the NPR. You should test several slot frequencies across the noise bandwidth—low, midband, and high.

The NPR is usually plotted on an NPR curve as a function of rms noise level referred to the peak range of the system. For very low noise levels, the undesired noise is primarily thermal noise and is independent of the input noise level. Over this region of the curve, a 1-dB increase in the noise level causes a 1-dB increase in the NPR. As the noise level increases, the amplifiers in the system begin to overload, creating intermodulation products that cause the noise floor of the system to rise. As the input noise increases further, the effects of overload noise predominate, reducing the NPR dramatically. FDM systems are usually operated at a noise-loading level a few decibels below the point of maximum NPR.

In a digital system containing an A/D converter, the noise within the slot is primarily quantizing noise when low values of noise input signals are applied. The NPR curve is linear in this region. As the noise input level increases, the hard-limiting action of the converter causes clipping noise to dominate.

In a practical A/D converter, any dc or ac nonlinearities cause a departure from the theoretical NPR. Although the peak value of NPR occurs at a fairly low input noise level (rms noise = 1/4 V_O, where $\pm V_O$ is the range of the A/D converter), the broadband nature of the noise signal stresses the device, and the test provides a good indication of its dynamic performance.

Theoretically, NPR readings should be independent of any particular slot frequency. However, because of increased nonlinearities for the higher input frequencies, the NPR readings in the higher slots tend to be lower.

NPR testing using DSP techniques

Using FFT analysis techniques, you'll find NPR measurements a real challenge. Consider the case where the record length is 1024 and the sampling rate is 20 MHz. The FFT of 1024 contiguous time samples would place a spectral component every 19.53 kHz (20 MHz/1024). Because the notch-filter slot width is approximately 4 kHz, the probability of a spectral component falling within the notch is very low.

To achieve reasonable data stability in the FFT NPR analysis, a number of samples must fall within the notch. If ten samples are within the 4-kHz notch, then the resolution of the FFT would need to be 400 Hz, necessitating a record length of 50,000 for a sampling

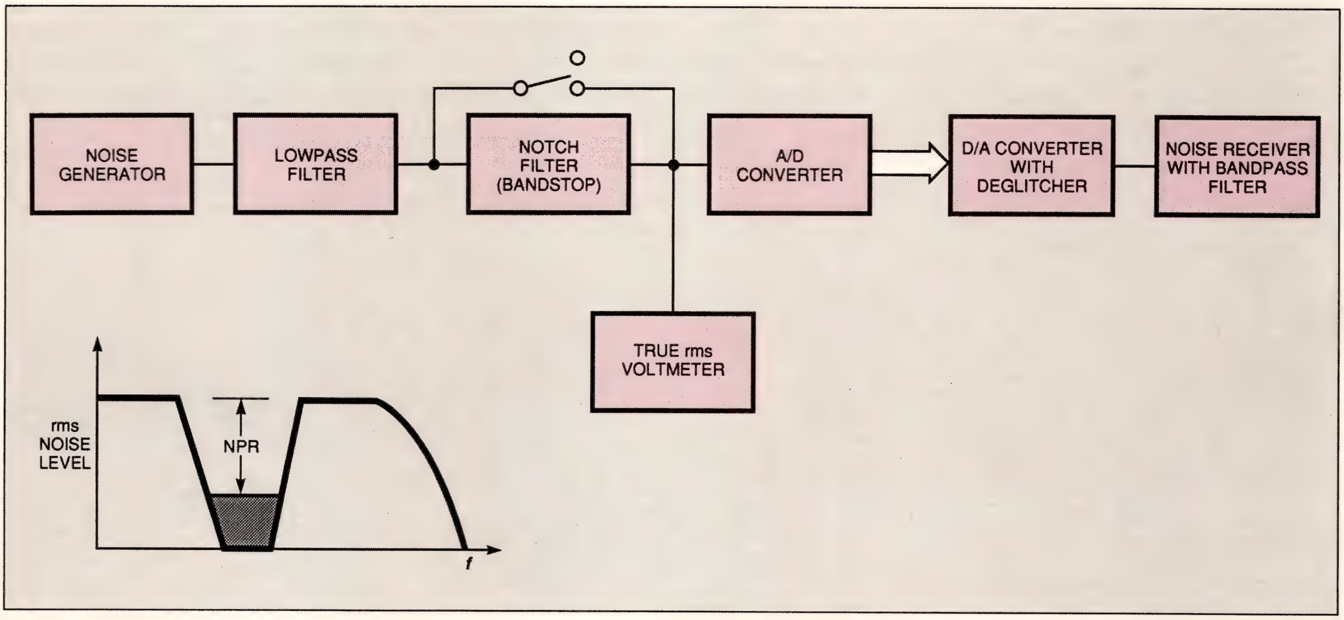


Fig 3—You can use this test setup to measure noise power ratio (NPR). *With the notch filter out, the receiver determines the noise power of the signal inside the notch. With the notch filter switched in, the receiver measures the residual noise inside the typical 4-kHz slot. The ratio of the two readings (in decibels) is the NPR.*

rate of 20 MHz. To avoid an extremely large buffer memory (and hence more demands on the FFT processor), you need to make the notch filter wider. For 20-MHz sampling and a 1024-word buffer memory, a notch filter that has a width of 200 kHz will provide ten frequency bins inside the notch. Even under these conditions, however, you should average the NPR calculations for several records to provide reasonable data stability.

Transient-response testing

The response of a flash converter to a transient input such as a square wave is often critical in radar applications. The major difficulty in implementing this test is obtaining a flat pulse that's commensurate with the converter's resolution.

A test setup for measuring the transient response of an A/D converter is shown in **Fig 4**. If you mount the Schottky-diode flat-pulse generator as close as possible to the analog input of the A/D converter, you can apply a signal to the A/D converter that's flat to at least 10-bit accuracy a few nanoseconds after it reverse biases the Schottky diodes.

You can use the same test setup to measure overvoltage recovery time. The amount of overvoltage is generally specified as a percentage of the A/D converter's range. For a converter with a 2V input range, 50% overvoltage corresponds to 1V above or below the nominal 2V input range. You make the starting point of the flat pulse correspond to the desired overvoltage condition. The actual recovery time is referenced to the time the input signal re-enters the A/D-converter input range. As in the transient-response test, you must consider the sampling (aperture) time delay when making this measurement.

The aperture-time and -jitter specifications of video A/D converters have probably been the least understood and most misused specifications in the entire field. The original concept of aperture time is centered around the classic S/H circuit of **Fig 5**. In an ideal S/H circuit, the switch has zero resistance when closed and opens instantly on receipt of an encode command. In practice, the sampling switch changes from a low to a high resistance over a certain finite time interval. An error occurs because the circuit tends to average the input signal over the finite time interval required to open the switch. As a result, the sampled voltage varies from the voltage at the instant the switch starts to open. The time required to open the switch is the aperture time. The error is determined by $E_a = t_a\ dV/dt$, where E_a is the aperture error, t_a is the aperture time, and dV/dt is the rate at which the input signal changes.

A simple first-order analysis, which neglects nonlinear effects, shows that no real error exists for such a switch. As long as the switch opens in a repeatable fashion, there is an effective sampling time that will cause an ideal S/H amplifier to produce the same hold voltage. The difference between this effective sampling point and the leading edge of the sampling clock is a fixed delay, which doesn't constitute an error. This effective aperture delay is the period from the leading edge of the sampling clock to the instant when the input signal equals the hold value. This specification

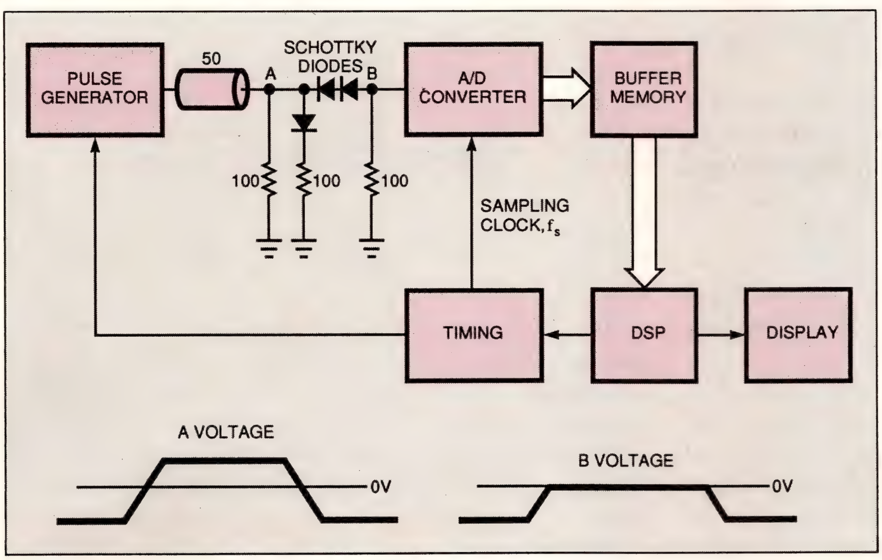


Fig 4—This test setup measures the transient response of an A/D converter. *The Schottky-diode network, located between points A and B in the circuit, generates a flat pulse for the input of the converter.*

In a practical A/D converter, the spurious-free dynamic range is a function of the converter's slew rate and can occur at a level below full scale.

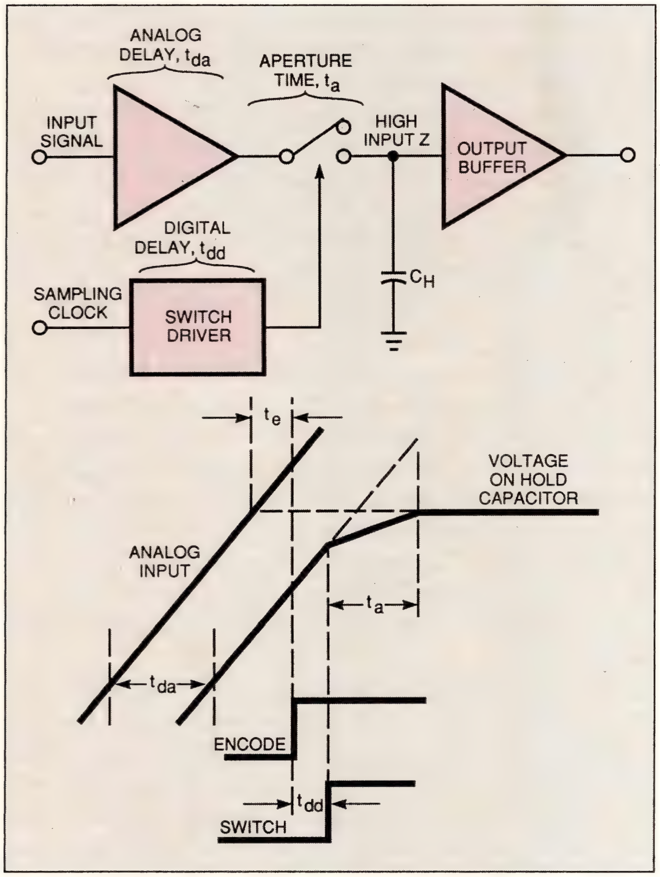


Fig 5—The concept of aperture time centers around the S/H circuit. *In practice, the sampling switch generates an error because of input-signal averaging over the finite time interval needed to open the switch. The aperture time is the time needed to open the switch.*

is important because it helps you determine when to apply the sampling clock with respect to the input signal timing.

The variation in effective aperture delay is important in simultaneous S/H applications. For example, in both I (in-phase) and Q (quadrature) radar receivers you may have to provide adjustable delays in the sampling clock to match the effective aperture delay times of several A/D converters. You should also consider delay-time tracking over a range of temperatures, especially in military systems where the specified operating temperature ranges from −55 to +125°C.

True aperture errors, however, do result from variable time delays. In a practical A/D converter, the sampling clock is often phase-modulated by some unwanted source; the source can be wideband random noise, power-line frequency, or digital noise due to poor grounding techniques. Phase jitter on the input sine wave can produce the same effect as jitter on the sampling clock. The resulting error is called aperture jitter. The corresponding rms voltage error caused by the rms aperture jitter qualifies as a valid aperture error.

The aperture-jitter specification is sometimes interpreted as a measure of the converter's ability to accurately digitize rapidly changing input signals. An A/D converter with an impressive aperture-jitter specification still may lose effective bits when digitizing a sine wave that has a maximum slew rate calculated from the aperture formula $E_a = t_a\, dV/dt$.

For example, assume that a 20-MHz, 8-bit flash converter has a bipolar input range of $\pm V_0$ ($2V_0$ p-p) and an aperture jitter specification of 20 psec rms. To calculate the maximum aperture-jitter error, convert the rms aperture jitter into a maximum value. If you consider that aperture jitter follows a Gaussian distribution similar to white noise, the rms aperture jitter, t_a, corresponds to the sigma (σ) of the distribution. The 2σ point on the distribution is a good place to set the maximum value, and the maximum aperture jitter becomes is $2t_a$.

If the corresponding maximum voltage error (ΔV) at the zero crossing of a full-scale sine wave is set to ½ LSB (½ LSB $= 2V_0/2^{N+1}$, where N equals the resolution of the A/D converter), then you can calculate the maximum full-scale sine-wave frequency, f_{max}, which will produce the ½ LSB aperture error, by using the following equations:

$$V(t) = V_0 \cdot \sin(2\pi f_t),$$

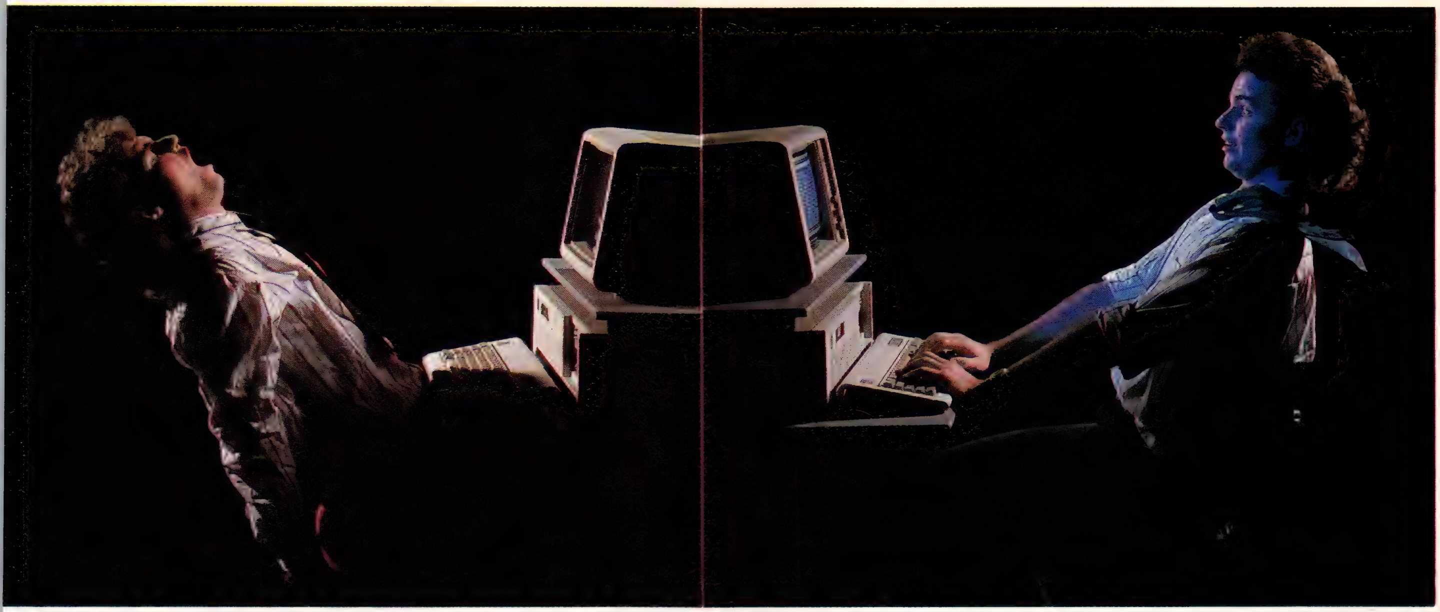
$$\frac{dV}{dt} = 2\pi f V_0 \cdot \cos(2\pi f_t),$$

$$\left.\frac{dV}{dt}\right|\max = \frac{\Delta V}{2t_a} = 2\pi V_0 f_{max}\Big|, \text{ and}$$

$$f_{max} = \frac{\Delta V}{4\pi V_0 t_a} = 2\pi t_a \cdot 2^{N+1}.$$

For $t_a = 20$ psec rms and $N = 8$, f_{max} is 16 MHz. These calculations imply that a 20-MHz flash converter can accurately digitize a full-scale sine wave of 16 MHz. In actual practice, however, the device may begin to suffer from skipped codes, decreased effective bits and S/N ratio, and ac nonlinearities at much lower frequencies.

You can calculate the effects of aperture jitter on



Histograms are useful in evaluating the differential nonlinearity of an A/D converter.

the full-scale sine-wave S/N ratio as follows:

$$V(t) = V_O \cdot \sin(2\pi f_t),$$

$$\frac{dV}{dt} = 2\pi f V_O \cdot \cos(2\pi f_t), \text{ and}$$

$$\frac{dV}{dt}\text{rms} = \frac{2\pi f V_O}{\sqrt{2}}.$$

For an rms error voltage, ΔV_{rms}, and an rms aperture jitter of t_a,

$$\frac{\Delta V_{rms}}{t_a} = \frac{2\pi f V_O}{\sqrt{2}}, \text{ and}$$

$$\Delta V_{rms} = \frac{2\pi f V_O t_a}{\sqrt{2}}.$$

The rms-signal to rms-noise ratio, expressed in decibels, is

$$\text{S/N ratio} = 20 \log\left[\frac{V_O/\sqrt{2}}{\Delta V_{rms}}\right]$$
$$= 20 \log\left[\frac{1}{2\pi f t_a}\right] \text{dB}.$$

The S/N ratio that's due exclusively to aperture jitter in the above equation is plotted in **Fig 6** as a function of the full-scale input-sine-wave frequency for various values of aperture jitter.

Consider an 8-bit, 20-MHz A/D converter with an rms aperture jitter of 20 psec. For an 8-MHz full-scale input, the S/N ratio due only to aperture jitter is 60 dB, as calculated from the equation. The theoretical S/N ratio due to quantizing noise in an 8-bit flash converter is 50 dB. When you combine the S/N ratio of 60 dB with the S/N ratio of 50 dB, you obtain a theoretical S/N ratio of 49.6 dB, which encompasses both the ideal quantizing noise and the noise due to aperture jitter. A practical 8-bit device that has an rms aperture-jitter specification of 20 psec may, however, only achieve an S/N ratio of 40 dB under these conditions.

Therefore, to accurately evaluate the A/D converter's dynamic performance, you must carefully examine the S/N ratio, effective number of bits, and aperture-jitter specifications.

Try measuring the aperture jitter of an A/D converter using the test setup shown in **Fig 7**. The low-jitter pulse generator produces both the sampling clock and the analog input signal to minimize the phase jitter between them. Adjust the phase shifter until the A/D converter repetitively samples the sine wave at its point of maximum slew rate at midscale. Then take a histogram on the digitized A/D-converter output data.

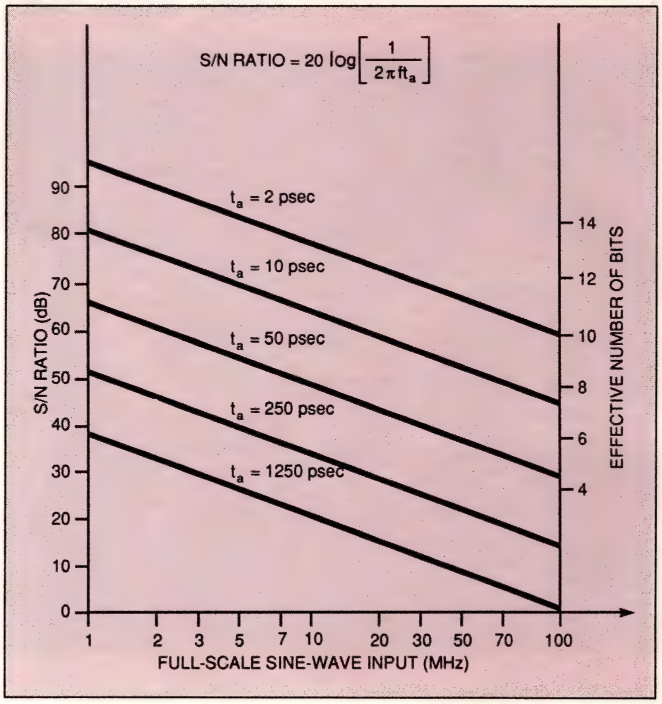


Fig 6—This plot compares the S/N ratio *to the full-scale sine-wave input frequency for various values of aperture jitter.*

An ideal A/D converter with no aperture jitter would have only one code present on the histogram. A practical converter gives a distribution of codes that you can fit to the normal distribution. The sigma (Σ) of the distribution corresponds to the rms error voltage, ΔV_{rms}, produced by the rms aperture jitter. Calculate the aperture jitter, t_a, from the formula

$$t_a = \frac{\Delta V_{rms}}{\frac{dV}{dt}}$$

where dV/dt is the rate-of-change of the sine wave at zero crossing.

If you sufficiently attenuate the input sine wave, any spreading of the distribution around the nominal code is due to intrinsic A/D-converter noise. As the input sine wave increases in amplitude, the slew rate, dV/dt, becomes proportionally greater, and the distri-

Noise-power-ratio tests are useful in determining the transmission characteristics of frequency-division-multiplexed communications links.

bution begins to spread because of the aperture jitter. Because high slew rates can affect the ac differential linearity of the converter, you should exercise caution when interpreting the histogram for high slew-rate inputs.

The offset adjustment shown in **Fig 7** lets you position the sine wave at different points on the A/D-converter range. In this way, you can see variations attributed to range-dependent differential-linearity characteristics. When offsetting the sine wave, make sure you don't exceed the A/D converter's input range.

It's also possible to measure effective aperture delay by using the locked-sine-wave technique. Adjust the phase shifter until the output reads midscale. Use a dual-trace scope to determine the difference between the leading edge of the sampling-clock pulse and the actual zero crossing of the sine-wave input. This difference is the effective aperture delay, which can be either negative or positive, depending on the values of the internal analog and digital delays in the S/H portion of the A/D converter.

At present, no industry standard exists for either the definition or the test for A/D-converter error rates. In flash converters, comparator metastable states can occur for low- or high-frequency input signals. At high frequencies, bubbles in the thermometer code of the comparator-bank output can also produce erroneous output codes.

Because error rates less than 1×10^{-16} are typical for well-behaved A/D converters, you need to take a large number of samples to properly measure the error rate. You must also take great care in the test-set layout, grounding, shielding, and power-supply decoupling so that 60-Hz, EMI, or RFI glitches don't create erroneous errors.

Use the circuit in **Fig 8** to measure the error rate for low-frequency input signals. Apply a low-frequency, full-scale sine wave (or triangle wave) to the A/D converter so that its rate of change is less than 1 LSB/sample. This step ensures that the transition zones between codes are all adequately exercised. An error amplitude of X LSBs is established as the lower limit for the definition of a qualified error. Usually, you select X to be several LSBs so that random noise doesn't produce errors. The software or hardware then examines the difference between each adjacent sample and records the number of times this difference exceeds the error threshold, X. If NQ is the number of qualified errors that occur, and NT is the total number of samples taken, then the error rate, ER, is given by the equation $ER = NQ/2 \cdot NT$.

As an example, consider an 8-bit, 100M-sample/sec flash converter designed to take at least ten samples at each code level. For one slope of the triangle-wave input, the number of samples required is $10\times256=2560$ samples. The frequency of the triangle wave is

$$f_t = \frac{1}{2560 \cdot 2 \cdot 10\ \text{nsec}} = 19.5\ \text{kHz}.$$

At a 100-MHz sampling rate, the average time required to make an error for an error rate of 1×10^{-9} is 10 seconds.

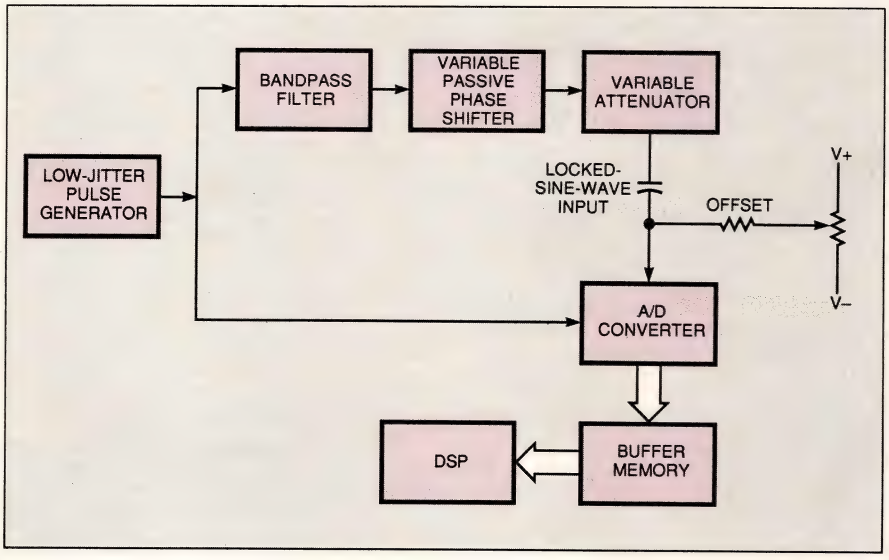


***Fig 7—In this test setup for measuring aperture jitter,** you adjust the phase shifter until the A/D converter repetitively samples the sine wave at its point of maximum slew rate. You then take a histogram of the digitized A/D-converter output data. The offset adjustment lets you position the sine wave at different points on the converter's range.*

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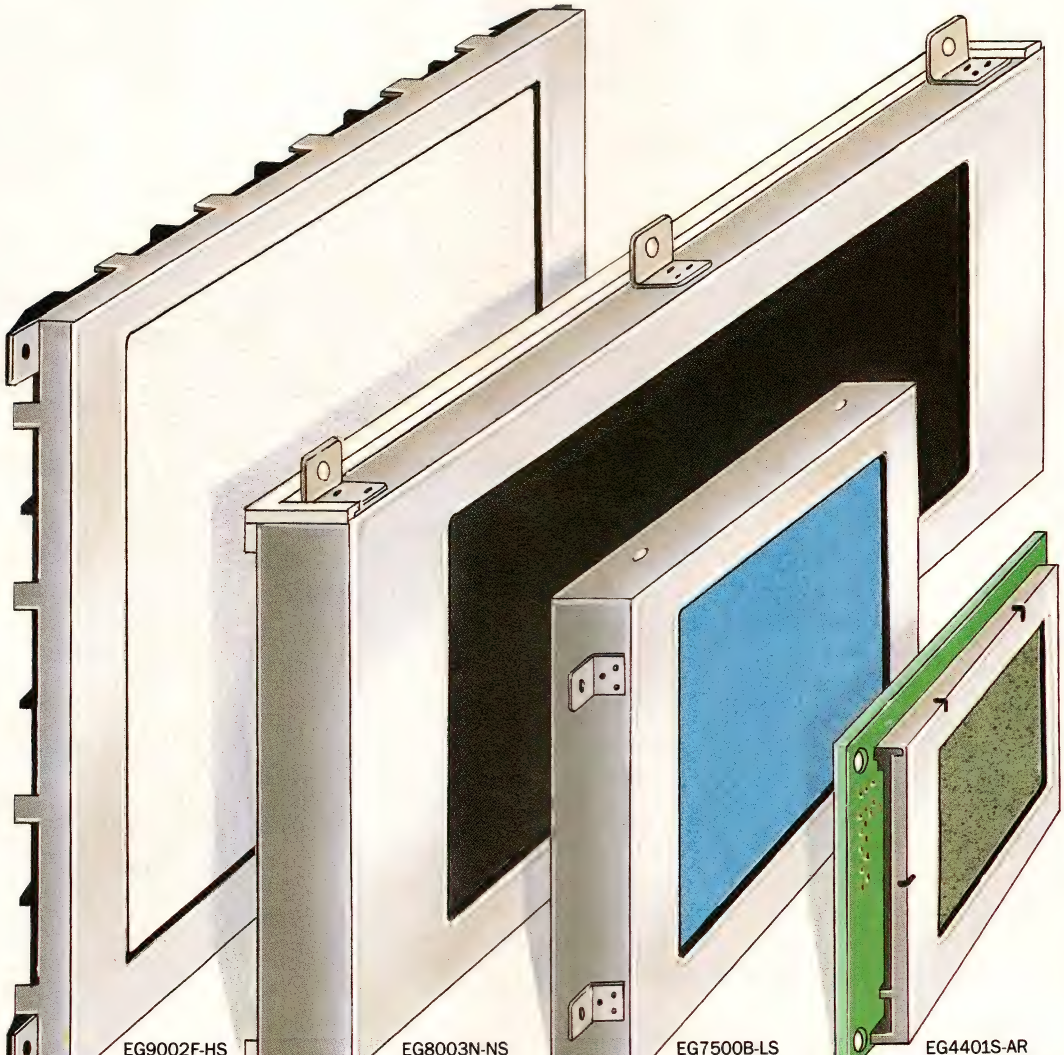

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CIRCLE NO. 56

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Aperture time and aperture jitter for A/D converters are probably the most misunderstood and misused specifications.

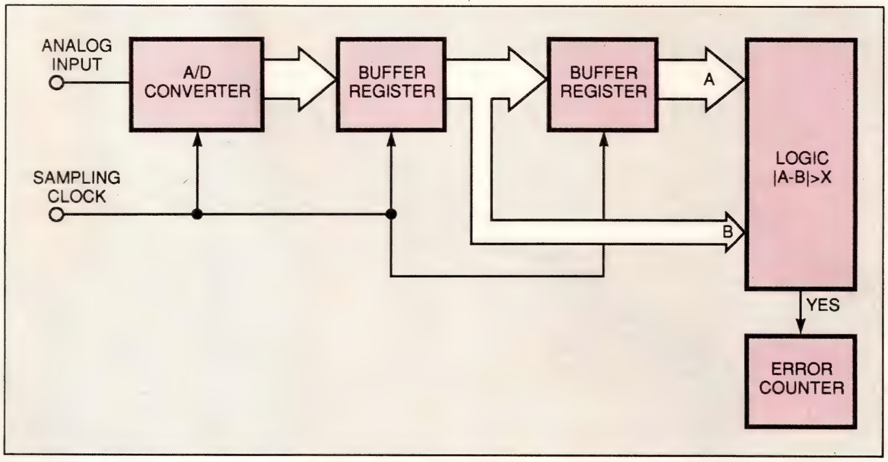

***Fig 8—The effective aperture delay** is the time difference between the leading edge of the sampling-clock pulse and the actual zero crossing of the sine-wave input.*

In a similar manner, you can measure dynamic errors caused by fast input signals by using the beat-frequency approach. You choose the low-frequency beat frequency to give the proper number of samples per code level, and then you examine the decimated digital outputs for adjacent sample differences that exceed the allowable error amplitude.

In summary, determining appropriate error-rate criteria for an A/D converter depends upon both the application and the characteristics of the converter under consideration. Flash converters that use straight binary decoding with no additional correction logic are most subject to large metastable errors at midscale. For this situation, a low-amplitude dither signal centered on the midscale code transition might be an appropriate stimulus. In a more well-behaved flash converter, a full-scale signal that exercises all codes might be desirable.

If you plan to digitize composite video signals, you'll need to measure the differential-gain and -phase performance of the flash A/D converter. Differential gain is the percentage difference between the digitized amplitudes of two signals. Likewise, differential phase is the phase difference between the digitized values of the same two input signals. The input signals are typically a high-frequency low-level sine wave representing the color subcarrier frequency, superimposed on a low-frequency sine wave. Distortion-free processing of the color signal requires that the flash converter alters neither the amplitude nor the phase of the chrominance signal as a function of the luminance-signal level.

The best method for performing composite video tests is to use an A/D converter back-to-back with a D/A converter. Connect a TV test signal to the A/D converter and use the output of the D/A converter to drive a vectorscope. To ensure that the test accurately measures the A/D converter's performance, use a low-glitch D/A converter followed by a track-and-hold deglitcher. In addition, the dc accuracy of the D/A converter should exceed that of the A/D converter. When testing an 8-bit flash converter, use a D/A converter with at least 10 bits of accuracy. EDN

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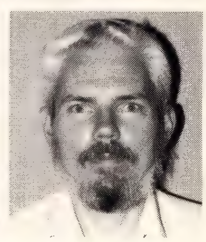
Author's biography



Walt Kester is a technical-support manager for the Computer Labs division at Analog Devices. Walt has been with the company for 20 years and supports the development of high-speed ADCs, DACs, S/H amplifiers, and op amps. He has a BSEE from North Carolina State University and an MSEE from Duke University. In his spare time, Walt enjoys carpentry and travel.

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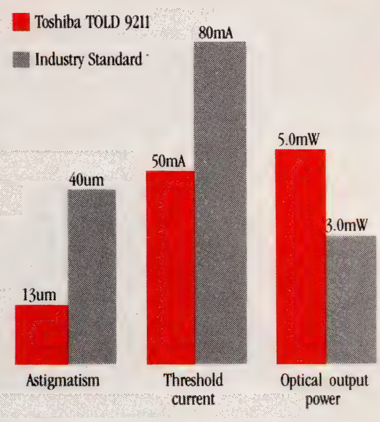

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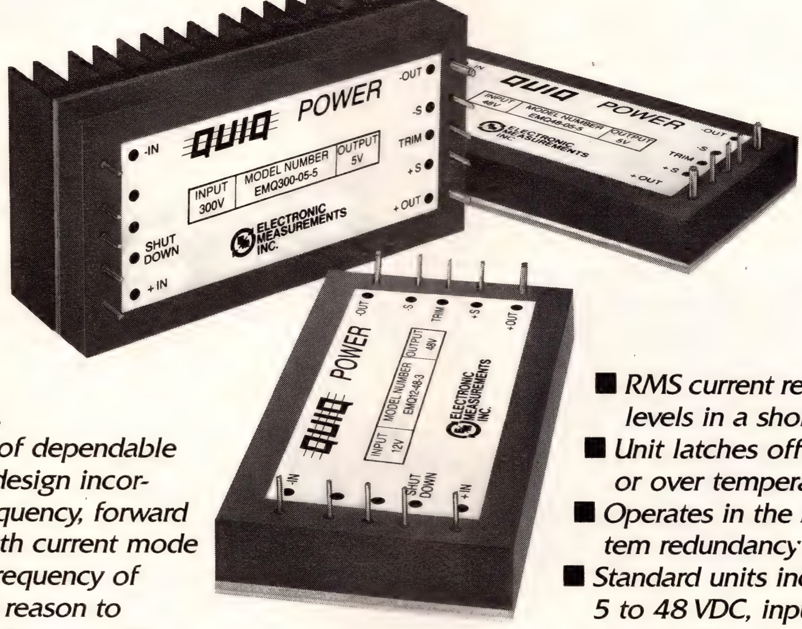

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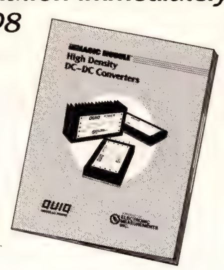

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News from Philips

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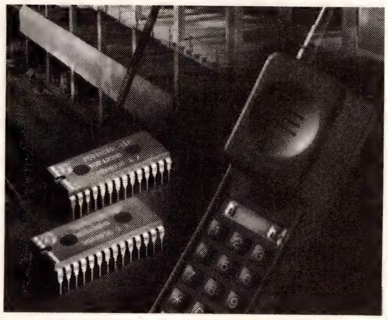
Philips enters SRAM market with ultra-low-power 64-kbit CMOS SRAMs

Philips Components is entering the byte-wide SRAM market with a high performance 8kx8 CMOS device offering ultra low-power consumption down to 1 μA both in 5 V standby and in the battery backup mode (V_{dd} = 3 V). Access times range from 55 ns to 70 ns. The 8kx8 CMOS SRAM is fully pin-compatible with devices presently on the market.



Philips Components' 64 kbit SRAMs suit many demanding applications.

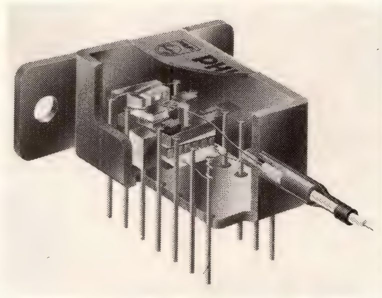
The new devices are manufactured in MOS-3, Europe's most advanced wafer fab based in Nijmegen, the Netherlands. The 1.2 μm, double-metal technology together with the full-CMOS six-transistor cell design account for the very low power consumption, very low sensitivity to alpha particles and wide operating temperature range. The FCB61C65 operates from a single 5 V supply; inputs and outputs are directly TTL- and CMOS-compatible. Two chip-enable pins are provided for maximum flexibility, easy memory expansion and controlling the standby mode. The address activated devices feature combined data input and output interfaces and can also be three-state controlled with a separate output enable pin.

The FCB61C65 normal and low power devices with an access time of 70 ns are available now in a 600 mil 28-pin DIL package and will be available in a 330 mil SO28XL package early 1990. The 55 ns part and the ultra low-power part will be offered in the near future.

Circle 14

InGaAsp laser diode for high bit-rate fibre-optic communications

Philips Components is introducing an ultra-fast DIL-pacakged InGaAsP laser diode for extremely high bit-rate fibre-optic communications. The CQF60 incorporates internal electrical compensation that allows operation at up to 2.4 GBits/s, a unique feature for a DIL-packaged laser diode. The LC compensation network counteracts the effects of the inductance and capacitance of the encapsulation and feed-through connections, provides perfect 50-Ω line impedance matching, and avoids electrical reflections.



1.3 and 1.55 μm wavelength lasers in user-friendly DIL package.

The 14-pin DIL package is both cost-effective and user friendly.

The CQF60 forms part of a new and comprehensive range of DIL-packaged InGaAsP lasers which covers the 1.3 μm and 1.55 μm wavelengths.

Circle 15

New ferrite helps lift SMPS operating frequency

Philips Components' 3F3 ferrite helps boost the operating frequency of switched-mode power supplies to 1 MHz, thus making the supplies smaller and lighter. The new ferrite will be attractive for EDP, aerospace, and telecom equipment, where size and weight are at a premium. It will work particularly well in new resonant-converter designs, which can furter reduce switching losses, increase operating frequencies, and cut EMI.

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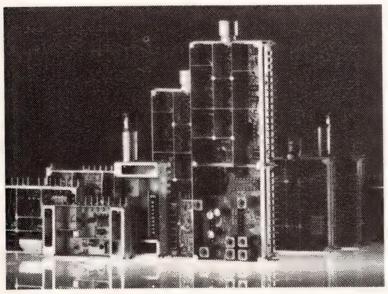
By reducing high-frequency losses, the ferrite reduces the core size without sacrificing power throughput. Replacing a conventional core with a 3F3 and simultaneously increasing the operating frequency from 50 kHz to 500 kHz leads to a threefold reduction in core volume and weight, and a tenfold reduction in the size of the output choke and capacitor.

Circle 16

TV tuners incorporate PLL tuning system

Philips Components has added two new series of TV tuners with built-in phase-locked loop (PLL) tuning systems to their range of VHF/UHF TV tuners. The UV-800 and UV-900 TV tuner series' advanced PLL tuning system contains all channel and function information necessary to control the tuner. In this way, a sizeable portion of external circuitry is made redundant, making CTV design both simpler and cheaper.



These PLL TV tuners make CTV design simpler and cheaper.

The PLL tuning system takes instructions from a microcomputer via the I²C Bus. The new ranges share the pinning and electrical configuration of the established Philips UV-600 and UV-700 series TV tuners, thus guaranteeing total compatibility throughout the range.

These tuners. They cover the entire TV broadcast spectrum in just three bands (VHF high, VHF low and UHF) in place of the four required for earlier tuner designs (VHF1, VHF3, Hyperband and UHF).

To further simplify system design, Philips also produces complete front-end modules. Housed in screened boxes slightly larger than those used for the tuners, these front-ends contain a tuner plus IF amplification and demodulation circuits, providing baseband video output with either quasi-split stereo or demodulated mono sound.

Circle 17

Clock-timer IC has low power consumption

The compact PCF8583 CMOS clock/timer/static RAM IC provides a wide range of timing functions, including a real-time clock with alarm functions, a calendar, and a timer or event counter.

Drawing typically just 10 µA from a 2.5 V to 6 V supply, the device is particularly attractive for normal telephones as well as for battery-operated and portable equipment such as pagers, remote handsets, and cordless telephones. A programmable timer or alarm interrupt allows the PCF8583 to reduce system power consumption by waking a processor from an idle mode at pre-programmed intervals.

With a resolution of 0.01 s, the PCF8583 works as a real-time 12- or 24-hour clock/calendar, keeping track of the year (with compensation for leap years), month, date, day of week, hour, minute, and second. As a timer, the PCF8583 provides elapsed time information in either days, minutes, seconds, or hundredths of a second.

The low-power PCF8583 provides a wide variety of timing functions.

The PCF8583 also has an on-chip 256-byte SRAM to store alarm, status or time information as well as telephone numbers, access codes, and other application-related information. The IC can connect to any microprocessor, and is controlled via the two-line I²C-bus. Its operating temperature range is −40 °C to +85 °C. Naked-chip versions are available, as well as versions in small outline and DIL packages.

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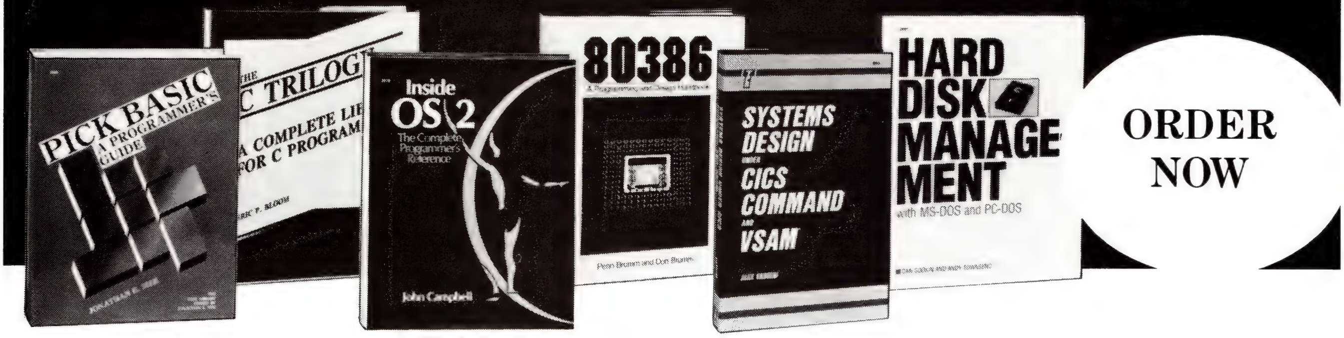

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Path-distribution analysis simplifies logic-circuit timing

Whereas logic simulators let you prove your circuit does what you want it to, timing-analysis CAD tools provide a more detailed examination of delay paths. Building a design from the results of a simulator without using a timing analyzer is like reading only the beginning of a story—you can't be quite sure how it will turn out.

Chi-Lai Huang and Marek Ryniejski, *Advanced CAE Div, Cadence Design Systems Inc*

Adding sophisticated timing-analysis capability to your logic simulator can help ensure that you have eliminated timing problems from your design before you commit to silicon. However, timing analyzers cannot automatically correct timing violations that exist in your design. Correcting violations requires engineering know-how and, often, considerable time. Nevertheless, a good timing analyzer does provide the tools to guide you quickly toward the optimum solution to timing-violation problems.

The path-distribution analyzer is an important tool in the timing-analyzer arsenal. When employing path-distribution analysis, you create a histogram of the number of arriving paths versus time for a given circuit. These plots give you a global view of the path timing and suggest the difficulty you'll face in attempting to improve circuit speed. You can use the path-distribution feature along with other timing-analysis tools to pinpoint specific changes that will improve circuit performance.

Definition of paths through gates

A review of path basics is in order before considering the use of path-distribution analysis. **Fig 1a** shows a simple inverter chain. You can use several different models to represent the output delays caused by input transitions on the inverter chain (**Fig 1b**). **Fig 1c** shows the output waveform for the simplest model, which assigns equal values to both the rise and fall delays. For example, assign each inverter a delay value of four units for both rising and falling output transitions. Here, the inverter chain's output transitions always trail input transitions by 12 time units (four time units for each of the three inverters).

A model allowing you to assign distinct delays for rising and falling output transitions provides more information than the simple 1-delay model. As an example, such a representation would allow assignment of a rise delay of six time units and a fall delay of two time units for each inverter in **Fig 1a.** These values would yield the output response in **Fig 1d.** For a 3-inverter chain, the total delay between a rising input transition and a falling output transition, $t_{FALL}=10$, is

Gates can have the same rise and fall times, different rise and fall times, or else they can use minimum and maximum values for their rise and fall times.

the sum of the fall delays for inverters G_1 and G_3 (two time units each) and the rise delay of G_2 (six time units).

Similarly, the total delay between a falling input and a rising output change for the inverter chain, $t_{RISE}=14$, is the sum of the rise delays of G_1 and G_3 (six time units each) and the fall delay of G_2 (two time units).

A representation that lets you assign either minimum or maximum delays for rising and falling transitions provides still more information. Consider, for example, assigning the following values for each inverter in **Fig 1a**: $t_{RISE(MIN)}=3$ time units; $t_{FALL(MIN)}=1$ time unit; $t_{RISE(MAX)}=7$ time units; and $t_{FALL(MAX)}=3$ time units.

Fig 1e shows a minimum total fall time of five time units (fall delays of one time unit each for G_1 and G_3 plus a rise delay of three time units for G_2). The minimum total rise time for **Fig 1e** is seven time units (rise delays of three time units each for G_1 and G_3 plus a fall delay of one time unit). **Fig 1f** shows a maximum total fall delay of 13 time units (fall delays of three each for G_1 and G_3 plus a rise delay of seven units for G_2). The maximum total rise delay is 17 time units (rise delays of seven each for G_1 and G_3 plus a fall delay of three for G_2).

The full adder in **Fig 2** illustrates timing analysis for a more complex circuit. Assume, for this circuit, that the NAND gate has minimum and maximum fall delays of one and three time units, respectively, and rise delays of two min and four max time units. The XOR gate, on the other hand, has fall delays of three min and five time units max and rise delays of four min and six time units max. The possible paths and delay times are

PATH	$t_{(MIN)}$	$t_{(MAX)}$
A-D-$C_{OUT(FALL)}$	3	7
A-D-$C_{OUT(RISE)}$	3	7
B-D-$C_{OUT(FALL)}$	3	7
B-D-$C_{OUT(RISE)}$	3	7
C_{IN}-F-$C_{OUT(FALL)}$	3	7
C_{IN}-F-$C_{OUT(RISE)}$	3	7
A-E-F-$C_{OUT(FALL)}$	6	12
A-E-F-$C_{OUT(RISE)}$	7	13
B-E-F-$C_{OUT(FALL)}$	6	12
B-E-F-$C_{OUT(RISE)}$	7	13
A-E-$SUM_{(FALL)}$	6	10
A-E-$SUM_{(RISE)}$	8	12
B-E-$SUM_{(FALL)}$	6	10
B-E-$SUM_{(RISE)}$	8	12
C_{IN}-$SUM_{(FALL)}$	3	5
C_{IN}-$SUM_{(RISE)}$	4	6.

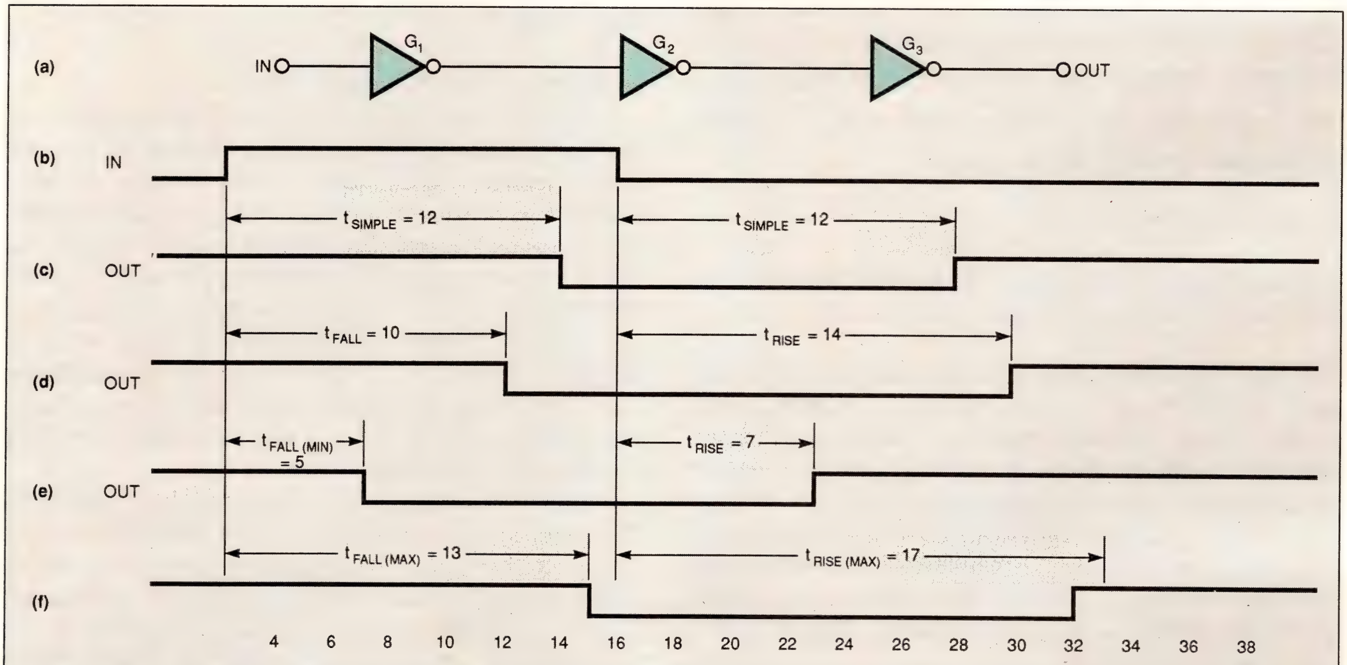


***Fig 1—For an inverter chain (a) driven by an input waveform (b)**, a timing analyzer can represent delays in any of three forms: as a single, typical delay value for both rising and falling outputs (**c**); as different delay values for rising and falling outputs (**d**); and, for both rising and falling outputs, as minimum (**e**) and maximum (**f**) delay values.*

The hybrid timing analyzer

Gateway's Veritime timing analyzer serves all logic-design applications—from integrated circuits to systems. It handles asynchronous as well as synchronous circuits. It can help users detect timing problems such as setup, hold, and minimum-pulse-width timing violations. The software also helps to correct these violations, in addition to predicting circuit performance before layout and tuning delay values to enhance circuit performance.

Veritime is a hybrid timing analyzer. The software gives you the option of combining static timing analysis with logic simulation. For circuitry with simple clocking schemes, you can use the static analyzer to find critical paths; whereas you can use the software's hybrid mode for designs with more complex timing.

For static timing analysis, you define begin and end points. You also specify the number of longest or shortest critical paths for the software to find and enumerate in one pass. Limiting the number of critical paths lets you isolate that part of the circuit where design changes can produce the greatest improvements in circuit performance.

KISS—Keep It Simple, Stupid

Complex clocking schemes often restrict your ability to perform static timing analysis. If your circuit uses multiple or multiphase clocks, then hybrid path tracing may be more helpful. With this feature, you employ your functional simulation patterns to exercise the clocking and control portions of the circuit. You also enable "timing checks"—that is, you specify nets at which the analyzer should check for timing violations. For example, you could specify the clock and data inputs of a flip-flop as the location of a potential setup violation.

When stimulus patterns cause value changes to propagate to clock/control inputs for which you've enabled timing checks, the software automatically initiates static analysis. For the flip-flop example, the software would find the critical paths to the data input and to the clock input. The software then compares the delay values to determine whether a setup violation exists.

An overly pessimistic analysis is one that would signal a timing violation based on theoretical worst-case analysis—even though actual conditions would prevent those worst-case conditions from occurring.

For example, consider two paths with stringent setup re1quirements with respect to each other passing through the same circuit component (a condition called reconvergent fanout). When looking for a setup violation, an overly pessimistic analyzer would assign a minimum delay to the component when calculating one path and a maximum delay to the same component when calculating the other path. The more realistic approach recognizes that a component can be either fast or slow; but not both. Therefore, a better analyzer restricts the delay-assignment range when reconvergent fanout exists.

Similarly, the software correlates gate delays on a substrate. The software won't assign the worst-case delay to some gates and the best-case delay to others when all the gates are on one chip. While there is likely to be some variability, to mix best- and worst-case delays on a single chip wouldn't reflect the relative consistency of IC processing. On the other hand, you can override this correlation for system-level timing checks.

In addition to this correlation, Veritime minimizes the adverse effect of feedback paths by automatically halting the tracing of loops that contain more than a user-specified number of logic gates. A default value of 10 allows the analyzer to exhaustively trace most common latches (which constitute "local" loops) while not tying up CPU time with exhaustive tracing of larger, "global" loops.

The vendor integrates the timing analyzer with their Verilog-XL logic simulator and Verifault-XL fault simulator. The timing analyzer shares the same hardware-description language of the Verilog family of products, which make up a complete range of verification and test tools, including libraries of software models as well as hardware-modeler support.

The number of possible paths through a circuit grows logarithmically as the number of gates increases, causing the analysis to become more complex.

The number of paths for this adder demonstrates how time consuming path-distribution analysis is for circuits of even moderate complexity. Consider that whereas a 2-bit multiplier contains 9.8×10^1 rising and falling paths from multiplicand to product, a 4-bit multiplier contains 3.6×10^4 such paths. Worse, the number of paths grows logarithmically so that a 28-bit multiplier contains 2.4×10^{38} rising and falling paths.

Clearly, exhaustive listing of circuit paths is not practical. Complete cataloging of even relatively simple circuits would yield more information than you could use. Consider that even an 8-bit multiplier has more than five billion paths.

Critical-path analysis provides micro view

Contrast the path-distribution analyzer with another timing-analysis tool, the critical-path analyzer. This tool finds and reports only a specified number of the slowest (or fastest) paths in a circuit, or region of a circuit. Some critical-path analyzers incorporate algorithms—called breadth-first—that quickly locate and report critical paths. Such analyzers are much faster than depth-first algorithms. (For more information on breadth- and depth-first algorithms, see **box**, "Timing-analysis algorithms.")

Nevertheless, breadth-first analyzers, too, can be inconveniently slow to use early in the design cycle. They can be inefficient because they may not indicate the severity of your timing problems. If you find paths with unacceptable delays, you cannot tell whether there are only a few or thousands of them. It may take hours before you determine that too many unacceptable delay paths exist. After investing this time, you may find that a complete redesign, or substitution of higher-speed parts throughout the design, is necessary.

Consider, for example, the full adder in **Fig 2**. Suppose you approach the problem without benefit of a path-distribution analyzer; you don't know how slow the slowest path is. A 1-path, critical-path search for the longest path would provide the delay and would note that the longest path could be A-E-F-$C_{OUT(RISE)}$. To find out that B-E-F-$C_{OUT(RISE)}$ exhibits the same delay, you'd have to start a second 1-path search. You could also conduct a multiple-path search, at the expense of CPU time, to find more than one of the slowest paths. At the fast end of the adder's performance, you'd have to conduct seven single-path searches—or one 7-path search—to uncover all seven paths with a minimal path delay of three.

Graphical display of path distribution, however, can quickly provide you with an overview of circuit timing. You can use standard workstations that incorporate the appropriate algorithms to generate such distributions in a reasonable amount of time.

A path-distribution histogram for the full adder shown in **Fig 2** would illustrate that two paths exhibit the longest delays of 13 time units. Furthermore, it would show that a total of six paths have delays of

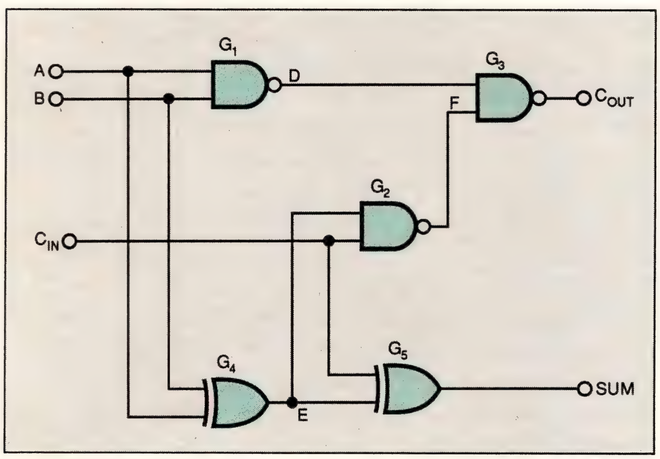


Fig 2—This simple adder has 16 paths from its three inputs to its two outputs, *demonstrating the difficulty of performing timing analysis for circuits of even moderate complexity.*

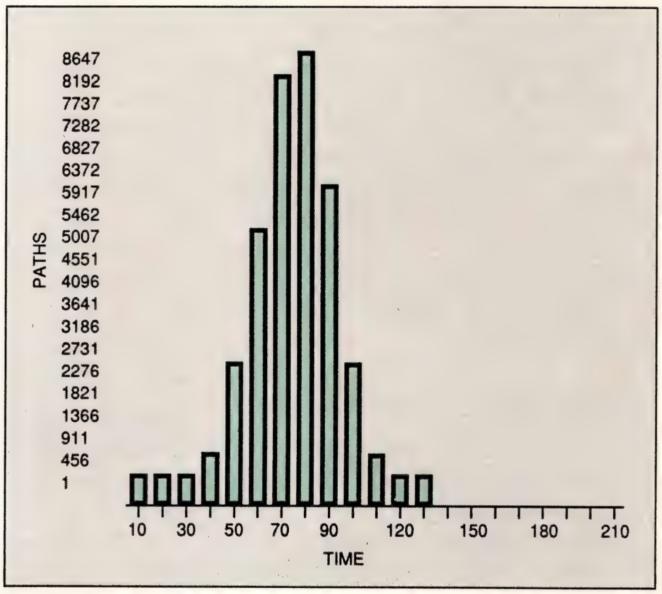


Fig 3—The path-distribution histogram for a 4-bit multiplier *suggests that it might be possible to eliminate all paths with delays of 120 time units or greater—if there are a reasonable number of such paths.*

Breadth-first timing algorithms tend to be faster than depth-first algorithms because the breadth-first approach avoids multiple tracing of a path.

more than 10. A user might then invoke a critical-path analyzer to search for the six longest paths, yielding the following results:

PATH	$t_{(MIN)}$	$t_{(MAX)}$
A-E-F-$C_{OUT(FALL)}$	6	12
A-E-F-$C_{OUT(RISE)}$	6	13
B-E-F-$C_{OUT(FALL)}$	6	12
B-E-F-$C_{OUT(RISE)}$	6	13
A-E-$SUM_{(RISE)}$	8	12
B-E-$SUM_{(RISE)}$	8	12.

In this simple case, notice that the XOR gate, G_4, is common to all of the slowest paths. Therefore, you can enhance circuit performance by using a faster XOR gate. This example shows the advantage of using both timing-analysis tools.

A histogram shows what is practical

Fig 3 shows a path-distribution histogram for a 4-bit multiplier. It illustrates that of more than 36,040 total paths, no path delay exceeds 140 time units. Note too that between one and 456 paths have delays greater than 130 time units, suggesting that you should further

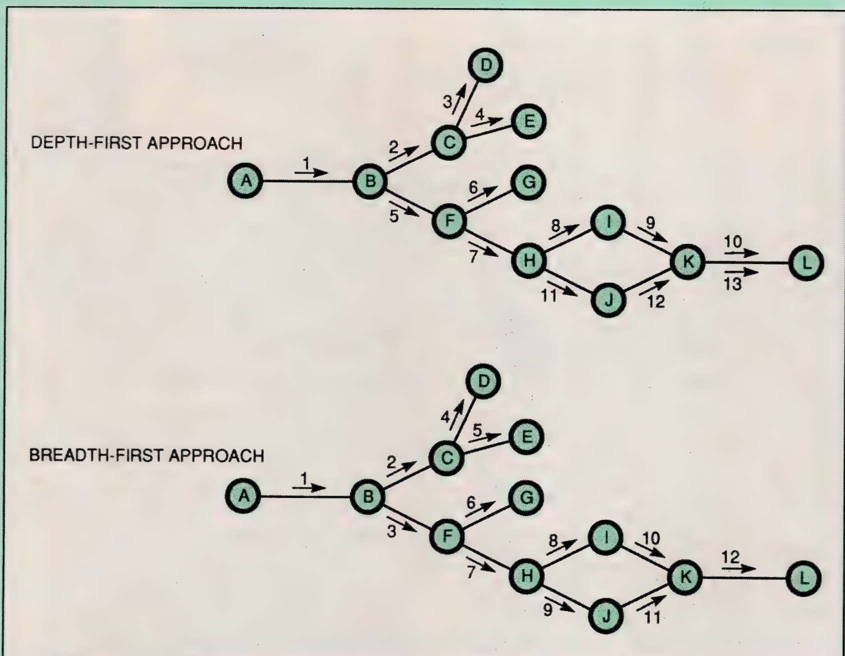
Timing-analysis algorithms

Timing analyzers typically use one of two algorithmic approaches: depth-first or breadth-first. To gain a basic understanding of how these approaches work, consider the two representations of a 12-node circuit shown in **Fig A**.

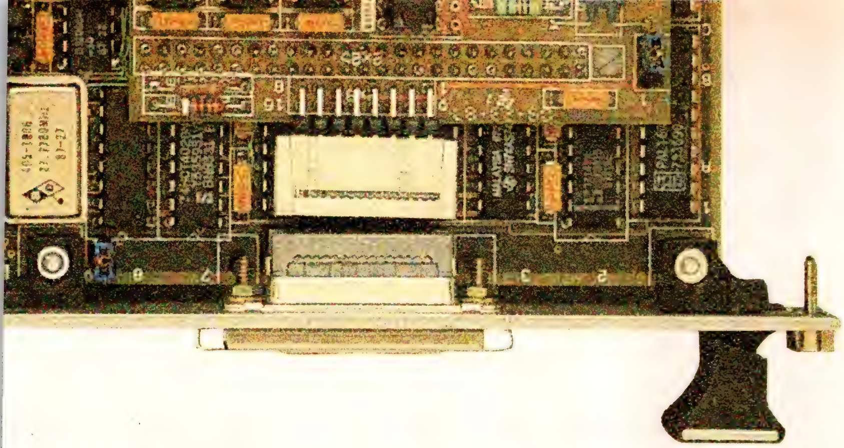
For the tree-like network, the depth-first algorithm explores a branch of the tree until the branch's termination; it then backtracks to the base of an unexplored branch and proceeds *from* there. For example, the depth-first algorithm first calculates the path A-B-C-D. Then it backtracks to node C to calculate path A-B-C-E; and then it backtracks to node B to calculate paths A-B-F, A-B-F-G, and A-B-F-H. From node H, it proceeds through nodes I, K, and L and then through nodes J, K, and L.

Note that the depth-first algorithm explores the path segment from K to L twice; once as part of path segment H-I-K-L and once as part of H-J-K-L.

The breadth-first algorithm improves analysis speed by avoiding such duplicate path explorations. It does not proceed from a node until it has calculated all paths *to* that node. For example, after calculating the delay to node K via node I, the breadth-first algorithm does not proceed to node L until it first calculates the delay to path K via node J. If the algorithm were searching for a longest critical path, it would add the delay of path segment K-L to the longer of the two delays (via node I or node J) to node K. The algorithm would discard the shorter delay to node K and the algorithm would not have wasted time performing an irrelevant calculation.



***Art A—Depth-first and breadth-first algorithms take different approaches to finding critical paths.** The circuit nodes (labeled A through L) illustrate the differences. The numbers along each path segment show the order in which the respective algorithms perform path-delay calculations.*



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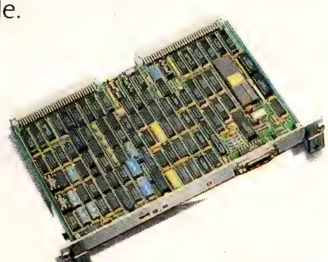

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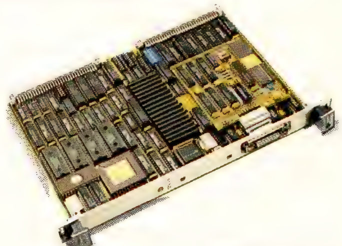

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NETWORKING SOLUTIONS

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CIRCLE NO. 64

Path-distribution analysis gives a macro view of your circuit's timing whereas critical-path analysis provides the micro view.

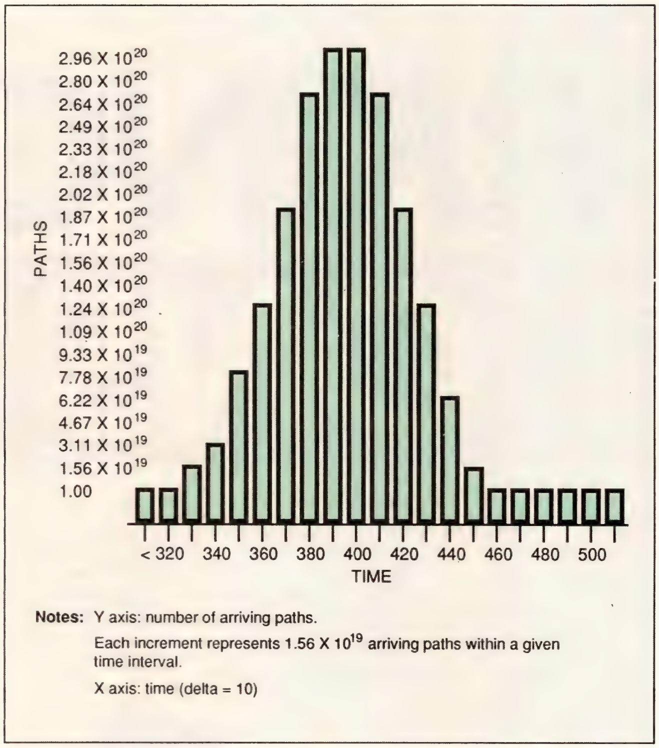


*Fig 4—**Although a 16-bit multiplier circuit contains more than 2×10^{21} paths,** the path-distribution software required only 227 seconds on a Sun workstation to provide a global picture of circuit timing.*

investigate whether you can reduce the maximum path delay to less than 130 time units. You would need to rerun the analysis with increased resolution to determine the feasibility of cutting the maximum path delays. Note, however, that it isn't practical to reduce the maximum path delay below 100 time units because of the existence of more than 2734 paths with delays longer than 100 units.

Timing analysis of a 16-bit multiplier illustrates the benefits of path-distribution capability in timing analysis. The alternative approach, using Gateway's Veritime critical-path tracer (running on a Sun 3/260 workstation), required 32 sec to run a 1-path trace, whereas a 4-path trace did little more than double the run-time to 66 sec. However, without benefit of the path-distribution analysis, you'd just be guessing at the number of paths to analyze.

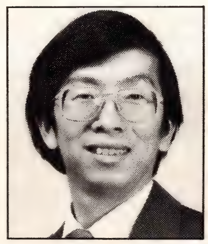
Searches for additional critical paths would take increasingly more time. Worse, you wouldn't know how much of the potential timing problem you'd analyzed, even after completing 10 or 20 path searches. Additional searches could yield many more paths with delays nearly as long as those of the paths already traced. Moreover, an exhaustive enumeration of such a circuit wouldn't be practical because the total number of paths from one operand to the 32-bit result exceeds 10^{20}.

In short, critical-path tracing alone can be time consuming and provides no information about circuit paths that you haven't traced. In contrast, path-distribution analysis provides global information about circuit delays in far less time. Veritime, for example, running on a Sun 3/260, generated the **Fig 4** histogram in 227 seconds.

The **Fig 4** histogram reveals the potential value of a 5- or 6-path trace to enumerate the few longest paths. The histogram also illustrates that additional traces to enumerate paths in the 450- to 460-time-unit range would be neither useful nor practical, thereby illustrating that path-distribution analysis is a powerful tool that complements critical-path tracing. EDN

Authors' biographies

Chi-Lai Huang has been with Gateway for 5 years. He earned his PhD in computer science at the State University of New York at Binghamton. Chi-Lai enjoys playing bridge and gardening.



Marek Ryniejski is a senior software engineer who is responsible for maintaining and enhancing Gateway's timing-analysis tool. He has a BA in computer science from Boston University. In his spare time, Marek enjoys cycling.

Article Interest Quotient (Circle One)
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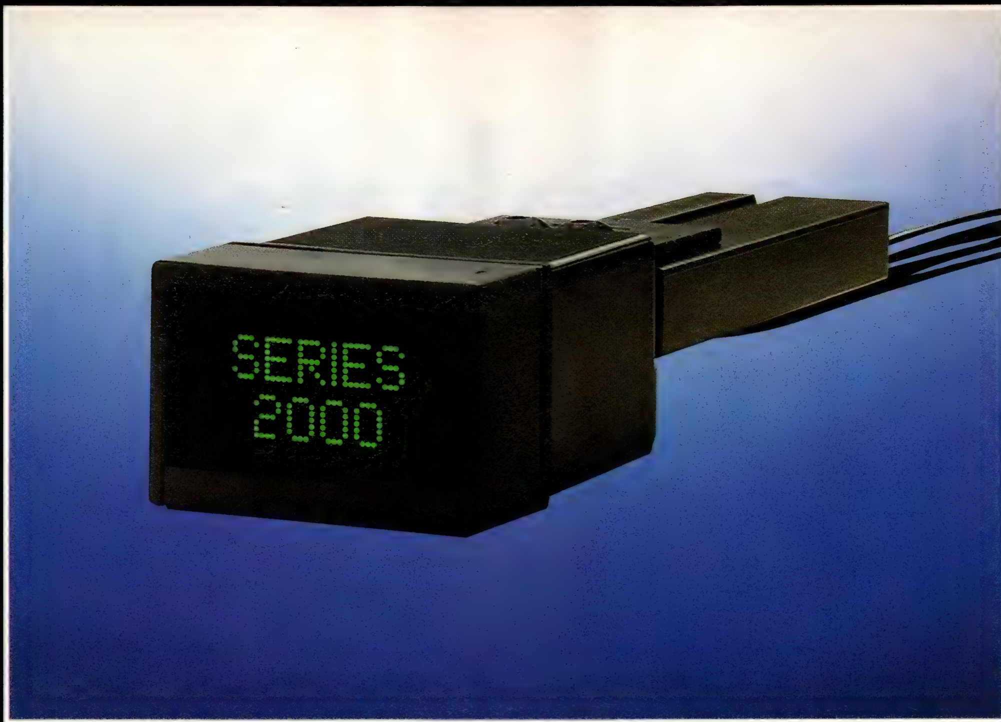

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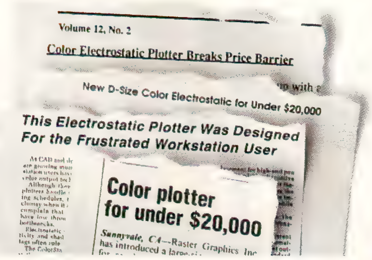

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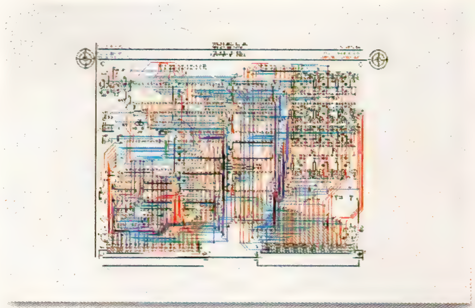

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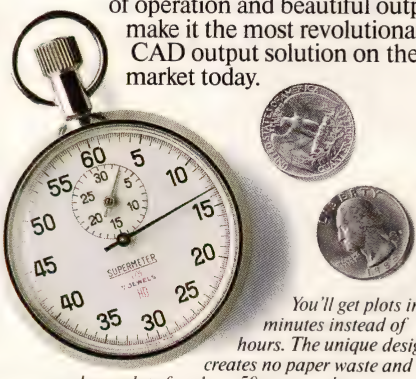

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February 19 Monday	9:00-11:00 AM	SCI TECHNOLOGY 5000 Technology Drive, Huntsville, AL
February 19 Monday	11:45-1:15 AM-PM	SCI TECHNOLOGY 8600 So. Memorial Parkway, Huntsville, AL
February 19 Monday	2:30-4:30 PM	INTERGRAPH CORPORATION Highway 20 - Intergraph Way, Huntsville, AL
February 20 Tuesday	8:30-10:00 AM	PENTASTAR ELECTRONICS INC. 5021 Bradford Blvd., Huntsville, AL
February 20 Tuesday	10:30-12:00 AM	UNIVERSAL DATA SYSTEMS 5000 Bradford Drive, Huntsville, AL
February 20 Tuesday	2:00-4:00 PM	ACUSTAR, INC., Huntsville Electronics Div. 100 Electronics Blvd., Huntsville, AL
February 21 Wednesday	8:00-10:30 AM	BOEING AEROSPACE 499 Boeing Blvd., Huntsville, AL
February 21 Wednesday	11:30-1:30 AM-PM	TELEDYNE BROWN ENGINEERING Sparkman Avenue, Huntsville, AL
February 21 Wednesday	2:30-4:00 PM	AVEX ELECTRONICS 4807 Bradford Drive, Huntsville, AL
February 22 Thursday	8:00-10:00 AM	SCIENTIFIC-ATLANTA, INC. 4311 Communications Drive, Norcross, GA
February 22 Thursday	11:00-1:00 AM-PM	AT&T Network Systems 2000 Northeast Expressway, Norcross, GA
February 22 Thursday	2:30-4:00 PM	BELL NORTHERN RESEARCH 5555 Spalding Drive, Norcross, GA
February 23 Friday	9:00-11:00 AM	NORTHERN TELECOM INC. 1555 Roadhaven Drive, Stone Mountain, GA
February 23 Friday	1:00-2:30 PM	HARRIS/LANIER, Voice Products 1704 Chantilly Drive NE, DeKalb, GA
February 26 Monday	10:00-1:00 AM-PM	HARRIS CORPORATION, Electronic Systems Palm Bay Road, Palm Bay, FL
February 26 Monday	2:30-4:00 PM	HARRIS CORPORATION, Controls & Composition John Rode Boulevard, Melbourne, FL
February 27 Tuesday	8:30-10:00 AM	IBM CORPORATION 1626 S. Congress Avenue, Del Ray, FL
February 27 Tuesday	11:30-3:30 AM-PM	IBM CORPORATION 1000 NW 51st Street, Boca Raton, FL
February 28 Wednesday	8:30-10:00 AM	MODULAR COMPUTER SYSTEMS (plant 8) 3101 S.W. 10th Street, Pompano Beach, FL
February 28 Wednesday	10:45-12:00 AM	HARRIS CORPORATION, Computer Systems Div. 2101 W. Cypress Creek Road, Ft. Lauderdale, FL
February 28 Wednesday	2:00-4:00 PM	RACAL-MILGO INC. 1601 N. Harrison Parkway, Sunrise, FL
March 1 Thursday	8:30-11:00 AM	ALLIED SIGNAL AEROSPACE, Bendix/King ATAD 2100 N.W. 62nd Street, Ft. Lauderdale, FL
March 1 Thursday	1:00-3:00 PM	ENCORE COMPUTER CORPORATION 1801 N.W. 66th Avenue, Ft. Lauderdale, FL
March 2 Friday	9:00-11:00 AM	LORAL DATA SYSTEMS 6000 Fruitville, Sarasota, FL
March 2 Friday	1:30-4:00 PM	E-SYSTEMS INC., ECI Division 1501 72nd Street No., St. Petersburg, FL
March 5 Monday	10:00-1:00 AM-PM	HONEYWELL, INC., Space & Strategic Avionics 13350 Highway 13 So., Clearwater, FL
March 5 Monday	2:00-4:30 PM	AT&T PARADYNE CORPORATION 8545 126th Avenue No., Largo, FL
March 6 Tuesday	8:00-10:30 AM	MARTIN MARIETTA CORPORATION 12506 Lake Underhill Drive, Orlando, FL
March 6 Tuesday	12:00-2:30 PM	MARTIN MARIETTA CORPORATION East Sandlake Road, Orlando, FL
March 7 Wednesday	9:00-11:00 AM	NCR CORPORATION 3325 Platt Springs Road, W. Columbia, SC
March 7 Wednesday	2:00-4:00 PM	IBM CORPORATION 1001 WT Harris Blvd. West, Charlotte, NC
March 8 Thursday	9:00-11:00 AM	ALCATEL NETWORK SYSTEMS 2912 Wake Forest Road, Raleigh NC
March 8 Thursday	2:30-4:30 PM	NORTHERN TELECOM INC. Perimeter Park Drive, RTP, NC
March 9 Friday	8:00-11:00 AM	IBM CORPORATION Research Triangle Park, NC
March 9 Friday	12:00-2:00 PM	NORTHERN TELECOM INC. Research Triangle Park, NC

DATE	TIME	SITE
March 9 Friday	2:30-4:00 PM	NORTHERN TELECOM INC. Northern Telecom Plaza, RTP, Inc.
March 12 Monday	9:00-11:30 AM	AT&T TECHNOLOGIES 204 Graham-Hopedale Road, Burlington, NC
March 12 Monday	1:00-3:30 PM	AT&T TECHNOLOGIES I 85 & Mt., Hope Church Rd., McKleinsville, NC
March 13 Tuesday	9:00-11:00 AM	GENERAL ELECTRIC COMPANY 1501 Roanoke Blvd., Salem, VA
March 13 Tuesday	1:30-3:30 PM	GENERAL ELECTRIC COMPANY Mountain View Road, Lynchburg, VA
March 14 Wednesday	9:00-11:00 AM	GENERAL ELECTRIC COMPANY US Route 29 North, Charlottesville, VA
March 14 Wednesday	1:30-4:00 PM	IBM CORPORATION 9500 Godwin Drive, Manassas, VA
March 15 Thursday	8:30-11:00 AM	E-SYSTEMS INC., Melpar Division 11225 Waples Hill Road, Fairfax, VA
March 15 Thursday	1:30-4:00 PM	E-SYSTEMS INC., Melpar Division 7700 Arlington Blvd., Falls Church. VA
March 16 Friday	9:00-10:30 AM	RACAL COMMUNICATIONS 5 Research Place, Rockville, MD
March 16 Friday	12:00-2:00 PM	FAIRCHILD COMMUNICATIONS & ELECTRONICS CO. 20301 Century Blvd., Germantown, MD
March 16 Friday	2:30-4:00 PM	HUGHES NETWORK SYSTEMS 11717 Exploration Lane, Germantown, MD
March 19 Monday	9:00-11:00 AM	LITTON SYSTEMS INC., Amecon Division 5115 Calvert Road, College Park, MD
March 19 Monday	1:00-3:00 PM	ALLIED SIGNAL AEROSPACE 9140 Old Annapolis Road, Columbia, MD
March 20 Tuesday	8:30-11:00 AM	ALLIED SIGNAL AEROSPACE 1300 E. Joppa Road, Baltimore MD
March 20 Tuesday	12:30-3:00 PM	MARTIN MARIETTA AEROSPACE 103 Chesepeake Park Plaza, Baltimore, MD
March 21 Wednesday	9:00-11:30 AM	WESTINGHOUSE ELECTRIC Intl' Airport, Baltimore, MD
March 21 Wednesday	1:00-3:30 PM	MARTIN MARIETTA CORP., Ocean Systems 6711 Baymeadow Drive, Glen Burnie, MD
March 22 Thursday	9:00-11:30 AM	WESTINGHOUSE ELECTRIC COMPANY 111 Schilling Road, Hunt Valley, MD
March 22 Thursday	2:00-4:00 PM	AAI CORPORATION York Road & Industry Lane, Cockysville, MD
March 23 Friday	9:30-12:00 AM	UNISYS CORPORATION, Tredyffrin Swedesford Road, Paoli, PA
March 23 Friday	1:30-3:30 PM	LEEDS & NORTHROP Sumneytown Pike, North Wales, PA
March 26 Monday	9:00-11:00 AM	GENERAL ELECTRIC Market & Delaware St., Camden, NJ
March 26 Monday	1:30-4:00 PM	GENERAL ELECTRIC, Astrospace Jct. Rt. 571 & Rt. 535, East Windsor, NJ
March 27 Tuesday	8:30-11:00 AM	AT&T BELL LABORATORIES 200 Laurel Avenue, Middletown, NJ
March 27 Tuesday	2:00-4:00 PM	AT&T BELL LABORATORIES Whippany Road, Whippany, NJ
March 28 Wednesday	9:00-11:00 AM	ITT Defense Communications 492 River Road, Nutley, NJ
March 28 Wednesday	12:30-2:00 PM	ALLIED SIGNAL AEROSPACE, Test Systems Route 46, Teterboro, NJ
March 28 Wednesday	2:30-4:00 PM	ALLIED SIGNAL AEROSPACE, Flight & Guidance Route 46, Teterboro, NJ
March 29 Thursday	9:00-11:00 AM	AIL SYSTEMS INC. Comac Road, Deer Park, NY
March 29 Thursday	12:00-1:30 PM	AIL SYSTEMS INC. 1 Walt Whitman Road, Melville, NY
March 29 Thursday	2:30-4:00 PM	NORDEN SYSTEMS 75 Maxess Road, Melville, NY
March 30 Friday	8:00-10:00 AM	GRUMMAN CORPORATION, Aircraft Systems Stewart Avenue, Bethpage, NY
March 30 Friday	11:00-1:00 AM-PM	GRUMMAN CORPORATION, Aircraft Systems Maxess Road, Melville, NY
March 30 Friday	2:00-3:30 PM	NORDEN SYSTEMS 500 Bi-County Blvd., Farmingdale, NY

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LTC1050	Single, Low Power	5μV	0.05μV/°C	1.6μVp-p	No	± 9V
LTC1051	Dual, Low Power	5μV	0.05μV/°C	1.5μVp-p	No	± 9V
LTC1052	Single, 7652 Upgrade	5μV	0.05μV/°C	1.5μVp-p	Yes	± 9V
LTC1053	Quad, Low Power	5μV	0.05μV/°C	1.5μVp-p	No	± 9V
LTC1150	Single, ±15V Operation	5μV	0.05μV/°C	1.8μVp-p	No	±18V

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CIRCLE NO. 68

EDITED BY ANNE WATSON SWAGER

Averaging increases µP's ADC resolution

Tuomas Koljonen and Jarkko Vuori
Data-Guider OY Inc, Espoo, Finland

Some single-chip microprocessors have built-in A/D converters. Because of their integration limitations, such converters, Motorola's MC68HC11 among them, usually only have 8 bits of resolution; others have 10 bits. You can extend the resolution using the method shown in **Fig 1**.

The method is based on theoretical aspects of the quantization process. If your analog signal is exactly half way between two discrete conversion levels, two consecutive conversions will, statisically speaking, yield two different results. You can calculate the mean of these results in order to attain a higher resolution result of the converted input signal. The method doesn't require that analog inputs lie only at the half-way point between levels. By adding a sawtooth wave-

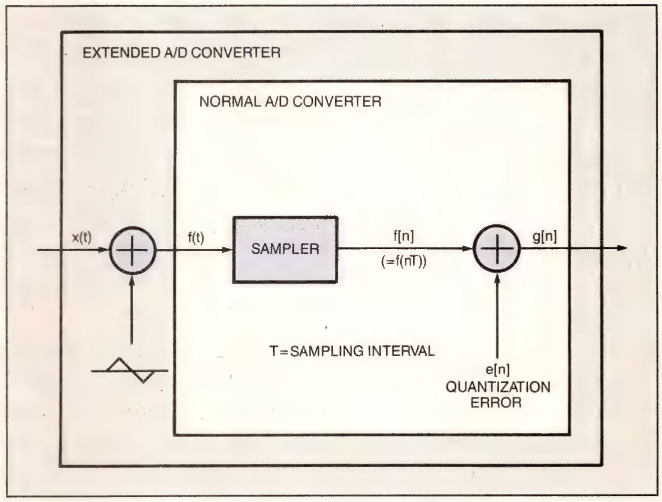

*Fig 1—**By adding a sawtooth waveform** to the analog input and then calculating the mean of a number of samples, you can extend the resolution of a µP's internal A/D converter.*

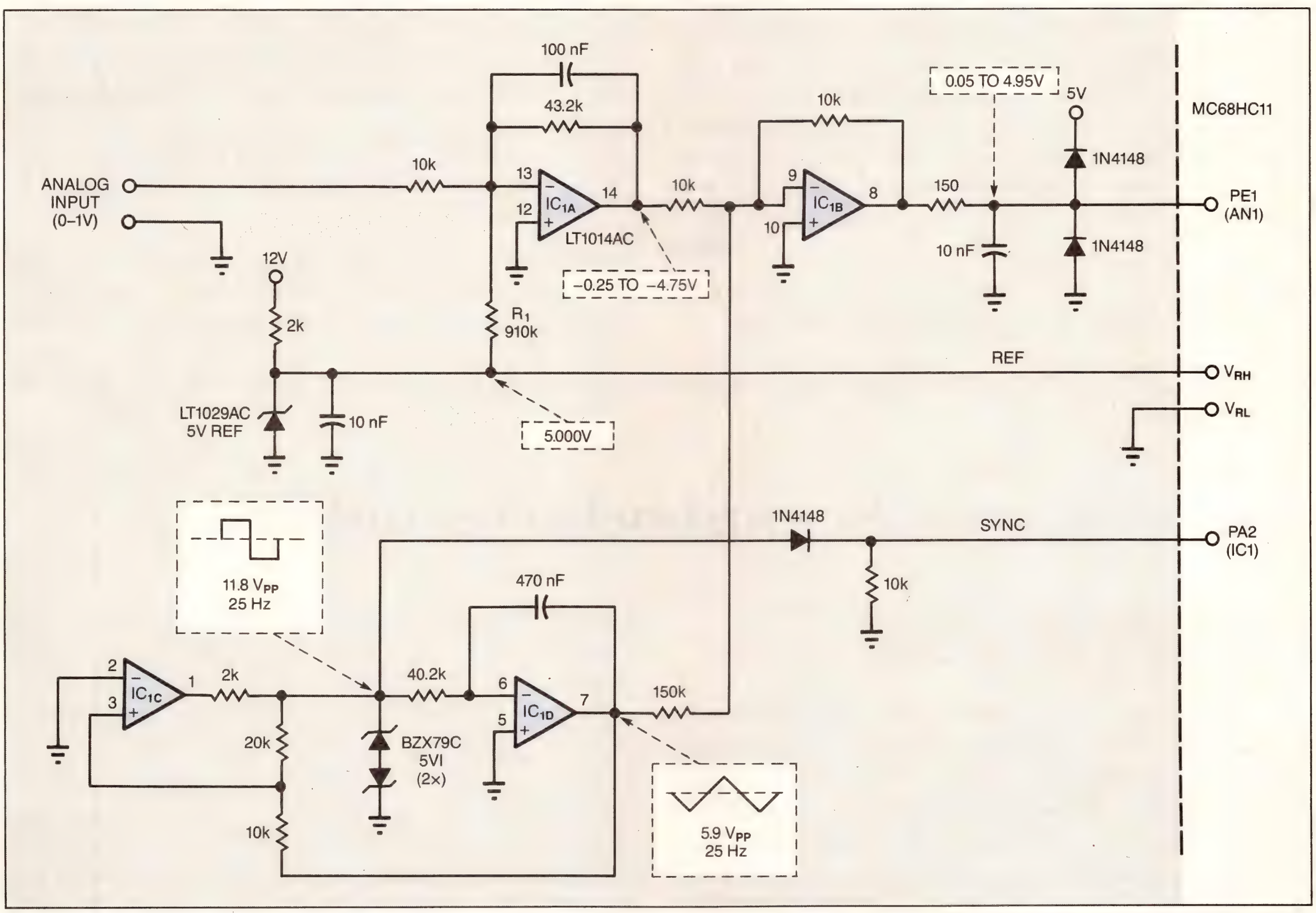

*Fig 2—**IC_{1B} combines the amplified and filtered input signal** with a $0.393V_{p\text{-}p}$ sawtooth waveform. Then the MC68HC11 takes the mean of a number of samples to yield a 12-bit result.*

form to the input signal, you can calculate the mean of a number of samples that occur within one or more sawtooth-wave cycles. The cost of the increased resolution time is a longer conversion time.

The circuit in **Fig 2** connects to the input of a M68HC11. The analog-input signal must lie between 0 and 1V, and the input impedance is 10 kΩ. IC_{1A} integrates and filters the input signal; this stage's cutoff frequency is 37 Hz. By adding a small input offset voltage at the input to IC_{1A} through R_1, the circuit prevents the final output from ever going negative. IC_{1B} adds the filtered input signal to the sawtooth wave and inverts the result. The output signal of the circuit, and thus the input to the MC68HC11, ranges from 0.05 to 4.95V.

You should set the value of the sawtooth wave's amplitude to around 20 times the smallest level difference of the converter. For example, an 8-bit, 5V converter would require 20(5/256), or 0.39V, as the p-p amplitude. The amplitude of the waveform at IC_{1B}'s input is 5.9(10k/150k), or 0.393 $V_{p\text{-}p}$.

You can write code for the MC68HC11 that calculates the mean of a number of consecutive samples using the flow diagram in **Fig 3**. Or you can write the authors at the following address for a listing of their M68HC11 interrupt-based resolution-extender program: Data-Guider Oy Inc, Visakoivunkuja 12 D 25, 02130 Espoo, Finland. The authors' program uses an algorithm that takes 128 consecutive samples, and uses them to calculate a 12-bit mean result. For a 12-bit result, the input-frequency-range limit is 0.78 Hz.

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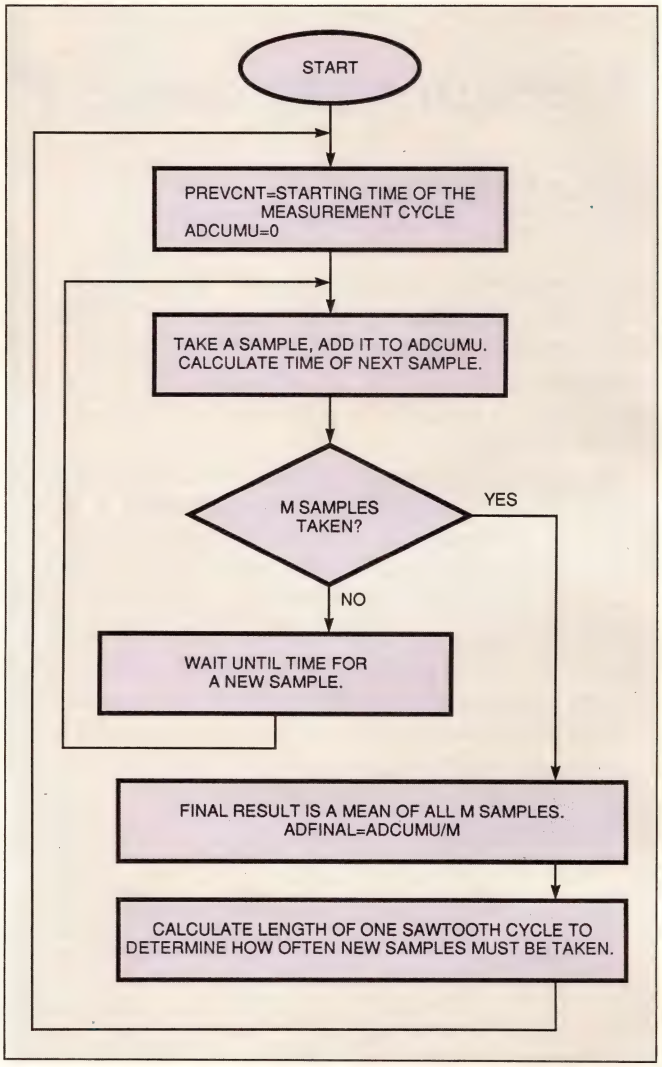

*Fig 3—**By writing code based on this flow diagram**, you can implement a resolution extender for the MC68HC11.*

Precision amplifier turbocharges buffer

Charles Kitchin and Fred Benkley
Analog Devices, Wilmington, MA

By combining a high-current buffer amplifier with a precision BiFET op amp, you can build a precise, high-current buffer amplifier **(Fig 1)**. Because the LM675 power op amp is inside the feedback loop of the AD711 BiFET op amp, the circuit exhibits the low input offset, low bias current, and low distortion characteristics of the AD711. With 10-kHz inputs, this circuit achieves a THD of less than 0.003% and a maximum offset voltage of 1 mV. The two op amps work well together because the AD711 has twice the slew rate of the LM675. Thus, the AD711 can quickly damp out any overshoots by the LM675.

You can configure the circuit as the high-input-impedance, unity-gain follower shown in **Fig 1**. Or, you can add a resistor to the overall feedback, add the input through a resistor to the inverting pin, and ground the noninverting pin of the AD711 to achieve a low-input-impedance inverting amplifier. The inverting-amplifier configuration has approximately 10 dB less distortion than the follower configuration; grounding the positive input eliminates the large amount of

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CIRCLE NO. 69

common-mode voltage that appears across the input terminals of an AD711 connected in a follower configuration.

The phase-lead network comprising C_1, R_3, and R_4 provides the necessary compensation to stabilize the response of the AD711 and LM675. You can tailor this network for your particular circuit application by trading bandwidth for phase margin (**Table 1**). The inverting circuit with a phase margin of 61° is stable when driving coaxial cable loads 100-ft long and resistive loads as low as 10Ω.

You can achieve the full 20W rms rating of the LM675 by running the LM675 from ±21V supplies and the AD711 from ±18V supplies. When you power both op amps from ±18V or ±15V supplies, the circuit can respectively provide 15 or 10W rms to an 8Ω load. Always include a 2- to 5-μF electrolytic capacitor on each power-supply line, and 0.1-μF capacitors at each amplifier's power-supply input. EDN

Table 1—Buffer-amplifier performance

R_3	R_4	C_1	Connection	Small-signal -3-dB bandwidth	Phase margin
4.02k	200	30 pF	Follower	1.77 MHz	35°
4.02k	100	68 pF	Follower	1.58 MHz	70°
4.02k	64.9	100 pF	Follower	1.34 MHz	86.3° *
4.02k	400	30 pF	Inverter	1.8 MHz	24°
4.02k	200	68 pF	Inverter	1.6 MHz	61°
4.02k	80	100 pF	Inverter	890 kHz	89.5° *

* Preferred connection for best transient response and highest stability

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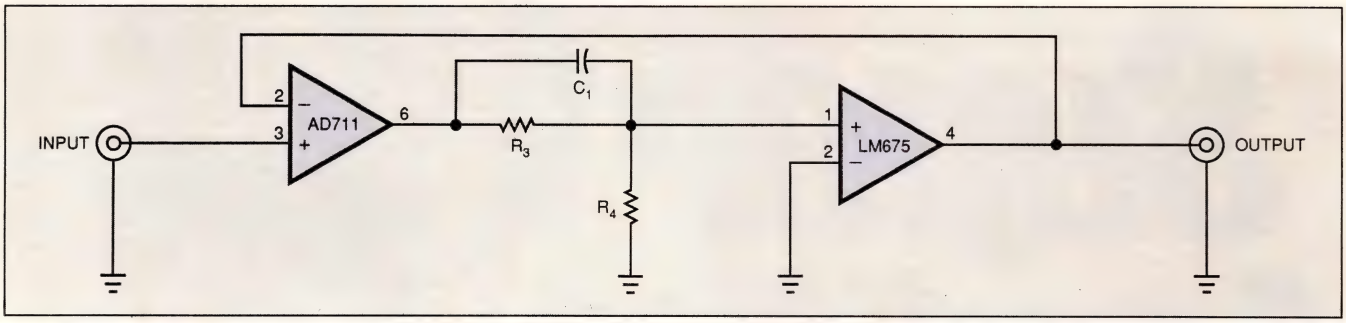

Fig 1—By matching the talents of two op amps, *this circuit can precisely drive high-power loads.*

Feedback enhances thermometer accuracy

T G Barnett
The London Hospital Medical College
London, UK

Fig 1's circuit measures body temperature by sensing both the temperature inside the ear's auditory meatus and the temperature of a heating pad inside an external heatset. By means of servo control, the circuit holds the heating pad's temperature approximately 0.2°C below the temperature of the auditory meatus. Thus, the heating pad minimizes the effects of the temperature outside the ear. The circuit implements a simple proportional controller, which operates in a slightly underdamped mode. Underdamping leads to small overshoots of pad temperature, which allow the circuit to reach the required temperature more quickly than if it were critically damped.

R_{T1} and R_{T2} are interchangeable R-T curve-matched thermistors with tolerances of ±0.05° over the 32 to 42°C temperature range. R_{T2} comprises a probe that you insert 10 mm into the auditory meatus. R_{T1} sits on the heating pad. Both thermistors are part of a Wheatstone bridge, whose output voltages differentially drive two LM363 precision instrumentation amplifiers. These amplifiers, IC_1 and IC_2, both have preset gains of 10. IC_1, the ear-probe amplifier, receives its signal from R_{T2}. IC_2, the heating-pad amplifier, receives its input signal from R_{T1}. Switch 1 feeds either amplifier output to a 20V full-scale digital panel meter so that you can read the ear-probe and heating-pad temperatures. You can trim the meter's gain to indicate a 100 mV/° change in the thermistor-sensed temperature.

Two different voltage dividers feed the two instrumentation amplifiers' sense pins. The dividers include 2-kΩ potentiometers, which are buffered by two op amps, IC_{3A} and IC_{3B}. You can adjust the potentiometers to offset the instrumentation amplifiers' outputs

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so that the meter reads the required temperature. For example, you can hard wire the meter's decimal point and adjust the potentiometer so that the meter reads 37.1°C when it senses 3.71V.

IC_{3C} and IC_{3D} together form a high-impedance differential amplifier with an overall gain of 23. The outputs of IC_1 and IC_2 drive the inputs to IC_{3D} and IC_{3C}, respectively. Note that a divider network, which includes a 5-kΩ potentiometer, attentuates the output of the heating-pad amplifier. By adjusting the potentiometer, you can adjust the set differential between the pad and the ear. The differential amplifier's output drives IC_4, a high-power op amp with a gain of 11 and a frequency response limited to 3.3 Hz.

The output of IC_4, in turn, drives the heating pad, which consists of a form of conductive rubber and has between 25 and 35Ω of resistance. The parallel LED indicates when power is on. For safety, the design attaches the pad to a thermal switch, which is set to open at 50°C.

You can power this circuit from a 12V rechargeable NiCd battery as shown in **Fig 2.** The 12V battery output directly powers IC_4, but the other op amps receive their power from three low-power precision reference sources. **Fig 2** includes a 50-mA antisurge protector to limit current under fault conditions.

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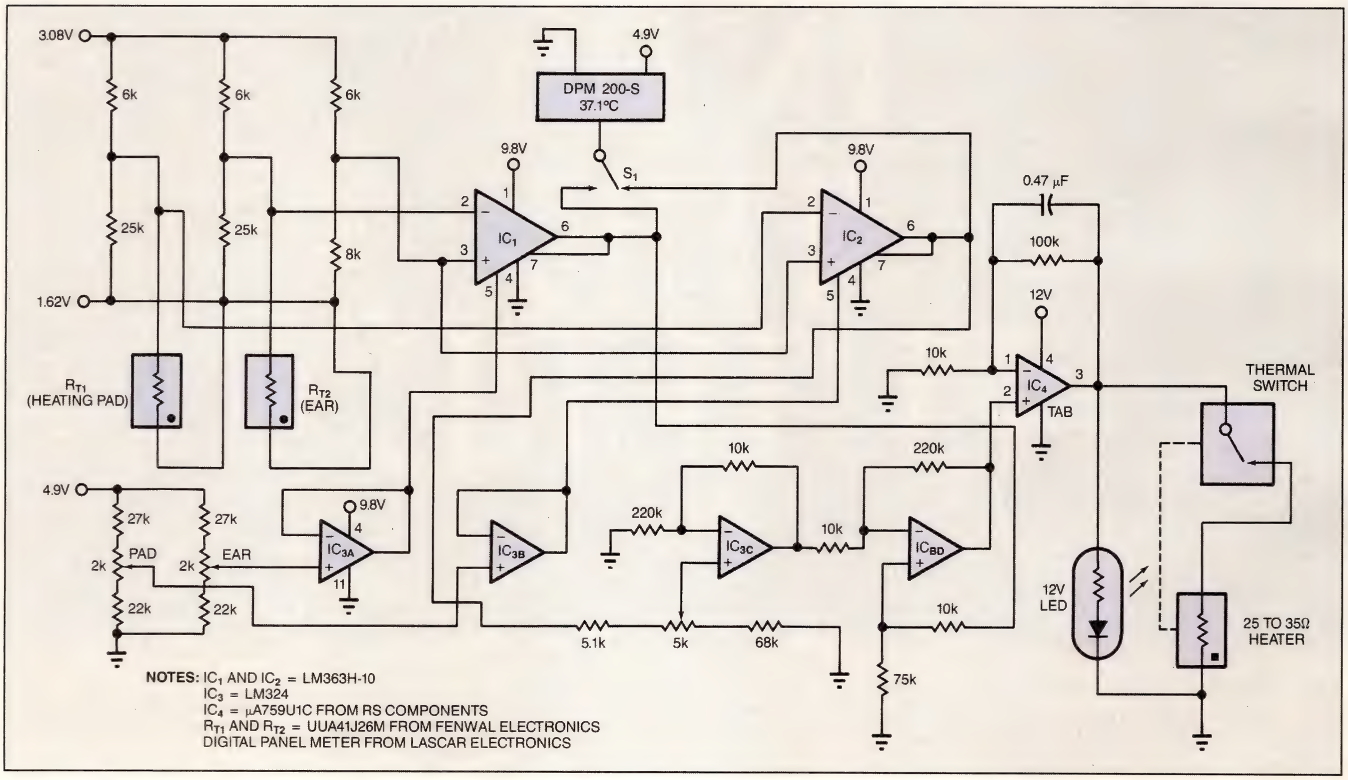


Fig 1—To accurately measure body temperature, *this control circuit maintains a small temperature difference between an ear probe and an over-the-ear heating pad. The heating pad minimizes the effects of external temperature conditions on the thermometer's measurement.*

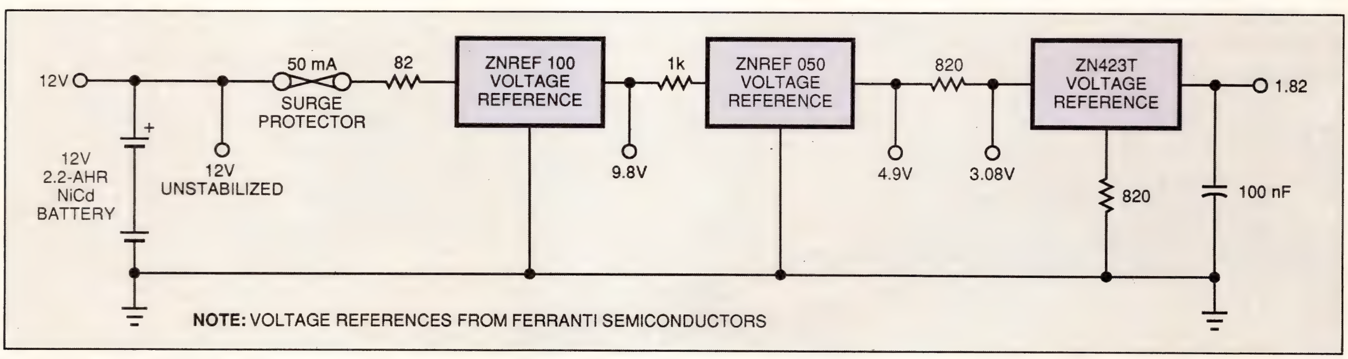
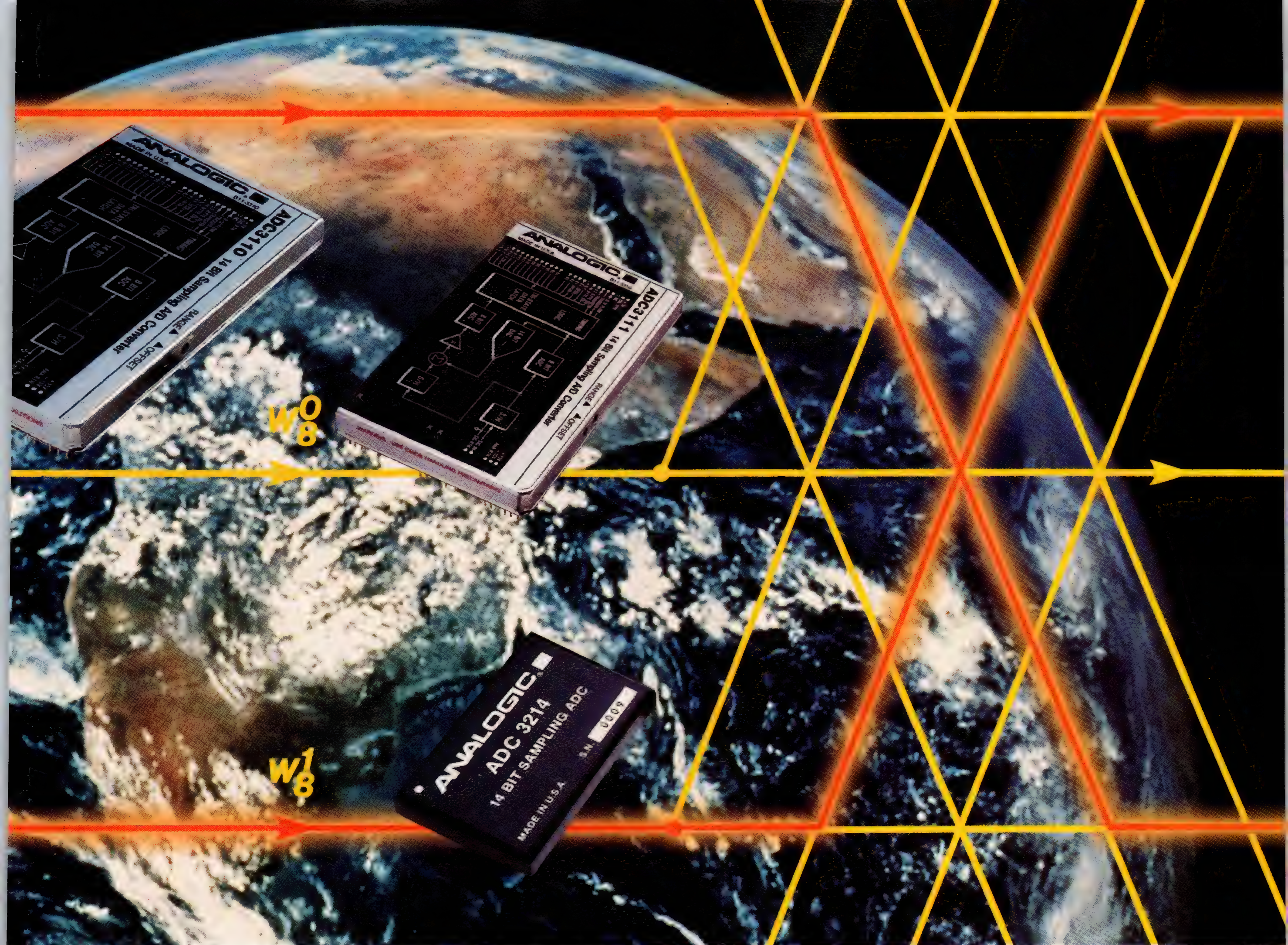


Fig 2—A 12V battery drives the output power amp, *but precision references power the circuitry used for actual temperature measurement.*



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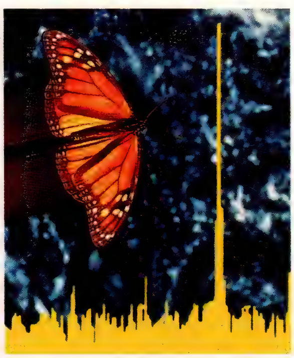

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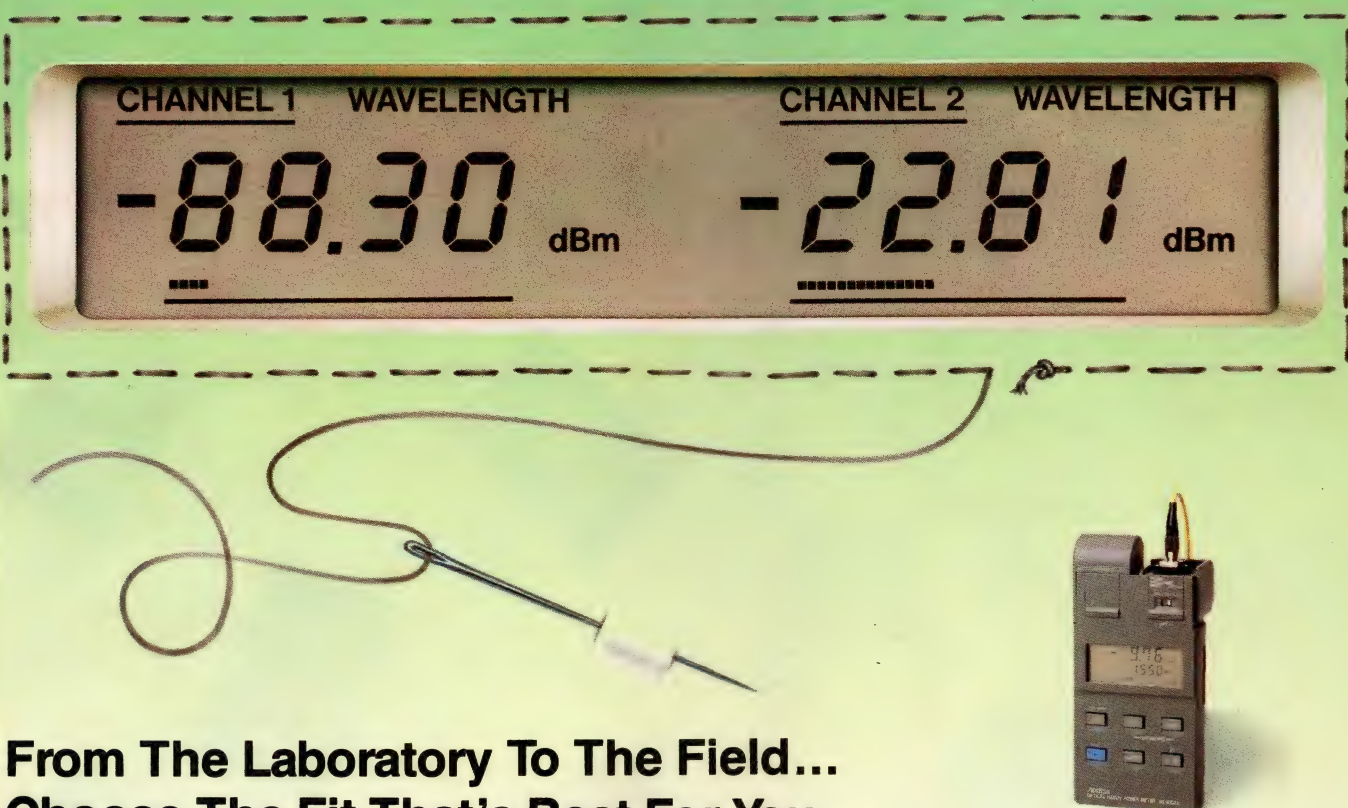

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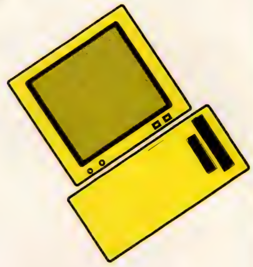

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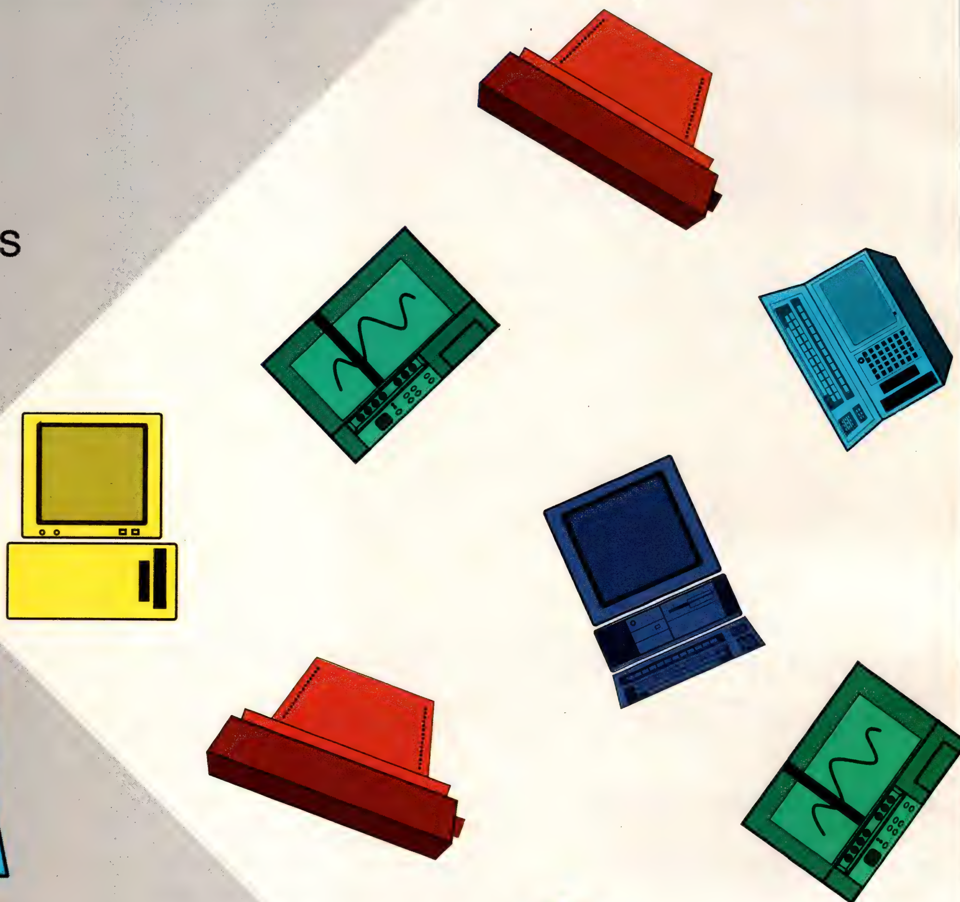

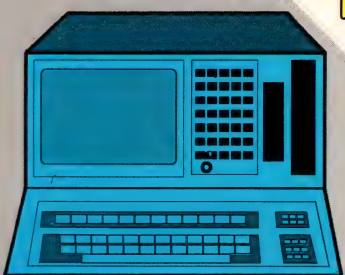

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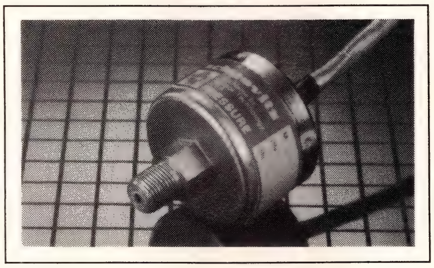

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- *Has a 4- to 20-mA output*

The Model 5081 2-wire pressure transmitter is compatible with data loggers and other instrumentation used in process control applications. The unit provides a 4- to 20-mA output from a 12 to 45V dc excitation; it offers both vented and sealed-gauge measurements over ranges of 0 to 5000 psi. Combined nonlinearity, hysteresis, and nonrepeatability are rated at ±1 FS output. Stainless-steel construction allows you to operate the unit in corrosive media. The unit is also water resistant. From $300.

Schaevitz Engineering, 7905 N Rte 130, Pennsauken, NJ 08110. Phone (609) 662-8000. FAX 609-662-6281. **Circle No. 370**

Bulk Power Converter

- *Has built-in power-factor correction*
- *Delivers 2100W*

The PM2958-6 bulk power converter uses 0.99 power-factor correction to meet stringent international safety and EMI standards. The unit operates from inputs of 90 to 264V ac and delivers an output

of 375 to 390V, which can be delivered to a PWM power supply or a distributed dc bus network. Depending on input voltage, the single-output converter will deliver a 1680 or 2100W output. Weighing 10 lbs, the unit is housed in a forced-air-cooled enclosure measuring 4×8×11 in. Operating range measures 0 to 50°C at full load. MTBF is calculated at 200,000 hours. Overvoltage and overtemperature protection are standard. $600 (OEM qty).

Pioneer Magnetics, 1745 Berkeley St, Santa Monica, CA 90404. Phone (800) 233-1745; in CA, (800) 848-1745. **Circle No. 371**

Common-Mode Filter

- *Meets FCC requirements*
- *Provides 20-dB attenuation*

The TRF-2000 tip-and-ring filter helps you meet FCC Part 68 requirements in 2-wire telecomm applications. The unit attenuates common-mode noise by 20 dB over a 30- to 250-MHz frequency range. Attenuation equals 15 dB to a frequency of 300 MHz. The filter has a 1500V isolation figure between windings, and dc resistance/winding equals 40 mΩ. Housed in a package measuring 0.4 in. square and 0.55 in. high, $1.50 (5000).

Coilcraft, 1102 Silver Lake Rd, Cary, IL 60013. Phone (708) 639-6400. **Circle No. 372**

4-Quadrant PWM Servo Amplifier

- *Has 100A current rating*
- *90% min efficiency*

The AD5020 4-quadrant PWM servo amplifier can drive servo motors with ratings as high as 50V. Continuous current ranges from 10 to 100A, and output ripple equals 140 mV max. Efficiency is 90% min, and standby power is 6.7W. Optocouplers and Hall sensors are used for isolation. Rotary switches with 10 positions ease the set-up process. A jumper allows you to configure the amplifier for either speed-loop or current-loop operation. A thermistor provides thermal protection. $446.

Zahn Electronics Inc, 2200 Northwestern Ave, Racine, WI 53404. Phone (414) 634-4300. **Circle No. 373**

4-Digit Programmable Displays

- *Available in three colors*
- *Operate to 100°C*

The IPD 4-digit, dot-matrix programmable displays are available in red (2545), green (2547), and yellow (2548). An 8-bit data word on the bidirectional bus supervises the

CMOS controller chip; the ASCII data and attribute data are word driven. Additional features include internal memory, decoders, multiplexers, and drivers. Viewing angle measures ±40 and ±75° for the X and Y axes, respectively. The TTL-compatible devices have a built-in character-generator ROM, read/write capability, and are easily cascaded to create larger displays. Software-controlled features include memory-clear function, lamp test, display-blank function, single- or multiple-character blinking, and three brightness levels. Operating range spans −55 to +100°C. $100 (100).

Siemens Components Inc, 19000 Homestead Rd, Cupertino, CA 95014. Phone (408) 725-3544.

Circle No. 374

Solid-State Thermostat

- *Monitors at the board level*
- *Has a ±1°C accuracy*

Housed in a 0.48×1.20-in. SIP, the TP Series solid-state thermostat monitors temperature at the board level. Designed for parallel or perpendicular mounting, the unit can trip at either one or two specified temperatures with ±1°C accuracy. The unit operates over a 2 to 65°C range and is available in normally open or normally closed versions for 5 to 24V dc operation. Compatible with most logic, relays, and indicators, the thermostat employs an open-collector npn transistor for the output. From $6 (5000).

Cambridge Aeroflo Inc, 900 Mt Laurel Circle, Shirley, MA 01464. Phone (508) 425-2346. FAX 508-425-2338.

Circle No. 375

Single-Turn Open-Frame Trimmers

- *Resistance values range to 1 MΩ*
- *Have a carbon element*

Model 3319 9-mm, single-turn open-frame trimmers have standard resistance values ranging from 100Ω to 1 MΩ. Housed on a ceramic substrate, the carbon resistive element is enclosed with a contaminant-resistant dust cover to increase life. The trimmers come with a choice of rotor colors (white is standard) and are available in side- or top-adjust models. Rated for 200 mW at 70°C, the units operate over a −25 to +100°C range. Contact-resistance variation equals 3% max, and temperature coefficient measures ±1000 ppm/°C. $0.20 (1000). Delivery, stock to 12 weeks ARO.

Bourns Inc, 1200 Columbia Ave, Riverside, CA 92507. Phone (714) 781-5500. TLX 676423.

Circle No. 376

NEW PRODUCTS

COMPUTERS & PERIPHERALS

3½-In. Hard-Disk Drive

- *Has an IBM PC/AT Type 17 intelligent interface*
- *Transfers data at a burst rate of 4.5M bytes/sec*

The KL343 3½-in. half-height hard-disk drive provides 42.5M bytes of formatted data storage. Its data-transfer rate is 4.5M bytes/sec in burst mode and 720k-bytes/sec rate in sustained operation. The drive employs an IBM PC/AT Type 17 intelligent interface and has an average seek time of 33 msec. The drive features independent DMA channels, error correction, sector-level defect handling, track and cylinder skewing, and a head autosleep mode. The device also contains an 8k-byte buffer between the host and the drive, which is expandable to 32k or 64k bytes. The MTBF is 40,000 power-on hours. The drive operates over a temperature range of 10 to 55°C. $495.

Kalok Corp, 1289 Anvilwood Ave, Sunnyvale, CA 94089. Phone (408) 747-1315. **Circle No. 358**

Bitbus Interface

- *Controls 250 devices for ISA bus computers*
- *Contains a 12-MHz 8044 μC and two 28-pin sockets*

The PC-Bitboss is a Bitbus interface board for the short slot in an ISA bus computer. The board can operate either as a master or as a slave. Operating as a master, it can control as many as 250 slave devices. The Bitbus Workbench software lets you control the Bitbus network using a windowed menu-driven format. You can send and receive messages, using the keyboard without writing code. The software drivers come in linkable source code that lets you incorporate them into an application program. The software also lets you download application programs to a specific node. A free application note and demo disk is available describing the software package. $372.

Computer Dynamic Sales, 107 S Main St, Greer, SC 29650. Phone (803) 877-8700. **Circle No. 359**

Memory Card

- *Plugs into the ISA bus*
- *Has access time of <160 nsec*

The PCard memory card plugs into the ISA bus and provides from 64k to 1024k bytes of storage with access times of <160 nsec. The product is available with static RAM, EPROM, or EEPROM storage devices. The PCard features dual-lithium batteries that can maintain data integrity as long as 10 years. Optional NiCad batteries are available for situations that require recharge. The card draws <55 mA from the host system and draws a maximum of 18 μA from the battery during standby mode. A battery-management system continually checks and reports on the battery condition. The board operates over −20 to +60°C and is available with an RS-232C interface. 64k-byte version, $98; 256k-byte version, $244.

Plus 5, 1640 5th St, #224, Santa Monica, CA 90401. Phone (213) 395-6076. **Circle No. 360**

1553 Bus Adapter

- *Includes a 68020 or 68030 μP*
- *Contains as much as 1M byte of dual-ported SRAM*

The Vx7-1553 adapter board for the VMEbus provides a communications path to the MIL-STD-1553 data bus. The board contains either a 68020 or a 68030 μP operating at speeds as high as 33 MHz. Options include either a 68881 or a 68882 coprocessor. In addition, the board has as much as 1M byte of zero-wait-state dual-ported static RAM (SRAM), two multiprotocol serial ports, and a configuration controller with timers. The 6U board can implement the bus controller, bus monitor, and remote terminal modes of the MIL-STD-1553 specification. The adapter can also accept special applications modules that allow you to add a VSBbus, SCSI, or Ethernet interface. Monitor and mailbox interrupts permit real-time processing. The single-slot board draws 3.1A from the 5V supply and a maximum of 50 mA from the ±12V supply. $3793.

General Micro Systems Inc, 4740 Brooks St, Montclair, CA 91763. Phone (714) 625-5475. FAX 714-621-4400. **Circle No. 361**

Display Controller

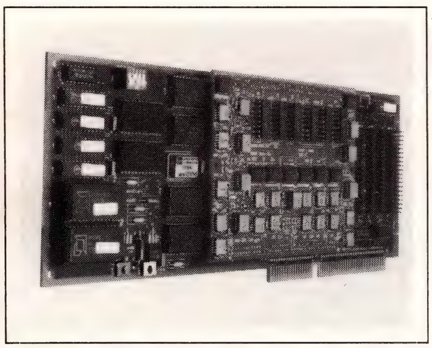
- *Has 1280×1024-pixel resolution*
- *Provides 256 simultaneous colors*

The VX8 graphics display controller card for the VMEbus provides 1280×1024-pixel resolution for color X Windows applications. The

card has 256 simultaneous colors from a palette of 16 million, and it refreshes a noninterlaced display at 60 Hz. Its graphics processor operates at 25 MIPS and can draw primitives as fast as 25M pixels/sec. In addition, the VX8 provides direct access to the frame buffer at a data-transfer rate of 20M bytes/sec for the host CPU or any bus master. The board translates 12-bit image data to 8-bit data before storage in the frame buffer and lets you view any quadrant of the frame buffer on a full-screen display. Other features include depth cuing and Gouraud shading for 3D applications. Optional X Server software for SunOS and VxWorks operating systems is available. $4950.

Jupiter Systems, 1100 Marina Village Pkwy, Alameda, CA 94501. Phone (415) 523-9000.

Circle No. 362



NTDS Interface Card

- *Connects to standard Navy computers*
- *Transfers 8-, 16-, or 32-bit data and half- or full-duplex devices*

The IOC I/O controller card for ISA bus computers provides a Naval Tactical Data System (NTDS) port for connection to standard Navy equipment. The card lets the computer simulate Navy computers such as the AN/UYK-7, -20, -43, and -44. The NTDS port conforms to the MIL-STD-1397A specification. Under program control, the card can transfer 8-, 16-, or 32-bit data and either half- or full-duplex devices. The card automatically configures itself to either the host's 8- or 16-bit bus. The IOC can execute either DMA or programmed I/O data transfers over the bus, and it can operate in either a polled or interrupt mode. In addition, the IOC has separate 512-byte FIFO buffers on the NTDS input and output ports as well as separate control, status, and word-count registers. $2900, including driver and diagnostic software.

Rockwell International Corp, Interface Products Group, Autonetics Marine Systems Div, BB44, 3370 Miraloma Ave, Anaheim, CA 92803. Phone (714) 762-1476.

Circle No. 363

CAE & SOFTWARE DEVELOPMENT TOOLS

Screen Generator

- *Lets you design data-entry and custom screens*
- *Can provide data validation for 17 types of data*

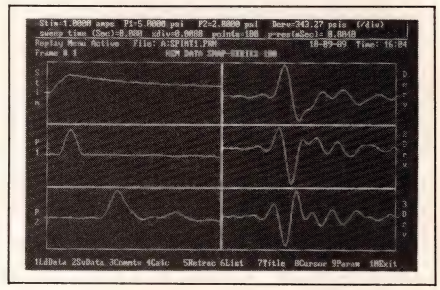
QuickScreen 3.0 is a screen designer for QuickBasic programmers. The program lets you draw text and backgrounds, define entry fields, and manage screen libraries that contain many screens in a single file. The package includes routines for field-by-field editing with full data validation of 17 different types of data. The program uses the same keystrokes as QuickBasic. You can store the screens that you create in any of three ways: as individual compressed-binary screen files; as object files that you can link with your application program; or in a screen-library file. The program gives you complete control over colors and highlights, and you can incorporate a variety of video effects such as horizontal or vertical wipes, dissolves, opening curtains, or roll-aways. $99.

Crescent Software Inc, 11 Grandview Ave, Stamford, CT 06905. Phone (203) 846-2500.

Circle No. 364

Screen-Printing Utility

- *Produces hard copy of a graphics screen display*
- *Can capture waveform displays to a disk file*



Snap-Print works with most data-acquisition or other application software that displays images on the screen and captures a screen display either to a disk file or to a hard-copy device such as a dot-matrix or laser printer. You can customize the printed-screen image by specifying the left and top margins on the page, the horizontal and vertical image size, draft or quality print, and whether black and white are to be reversed during printing. If you direct the output to a disk file, you can later merge the image into text generated by a word processor. The program is compatible

Text continued on pg 160

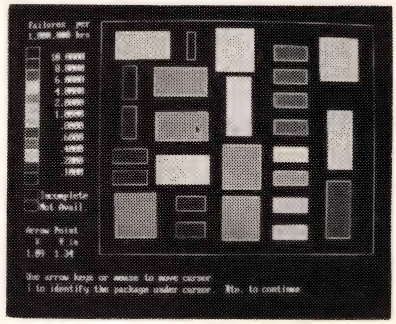
with IBM CGA, IBM EGA, IBM VGA, and AT&T 6300 monochrome graphics boards. $195, if purchased separately; $150, if purchased with one of the vendor's other products.

HEM Data Corp, 17336 Twelve Mile Rd, Suite 201, Southfield, MI 48076. Phone (313) 559-5607. FAX 313-559-8008. **Circle No. 365**

Thermal-Reliability Analyzer

- *Can evaluate boards of irregular shape*
- *Can interface with any CAD system*

The BETAsoft software package runs on IBM PCs and compatibles and predicts the thermal performance of a pc board, using parameters contained in a library of more than 2500 ICs and heat sinks. The program creates a 3-D thermal model of the board and can handle as many as 800 components (including surface-mount types) on each side of the board; the maximum number of types/board is 400. The program can handle natural or forced cooling, or a combination of both. The finite-difference algorithm takes into account the complex airflow and thermal fields caused by components of different sizes and heights, and incorporates reliability predictions. Upon completion of the initial calculations, the program displays the board temperature and the individual temperatures of components and IC junctions; you can relocate overheated components or add heat sinks, and then obtain a new display. You can direct any display to a plotter for hard copy, and obtain a reliability analysis that's compatible with the MIL-STD-217E standard. To run the program you need an IBM PC, PS/2, or compatible that has at least 320k bytes of memory (640k bytes recommended), an EGA-compatible display, and a hard disk. A math coprocessor is not required but will increase the computation speed. With one CAD-system interface (P-CAD, AutoCAD, PADS-PCB, Racal-Redac, or other), $2995.



Dynamic Soft Analysis Inc, 213 Guyasota Rd, Pittsburgh, PA 15215. Phone (412) 781-3016. FAX 412-781-3098. **Circle No. 366**

Logic Compiler For PLDs

- *Accepts input from schematic-capture program*
- *Compiles complete design rather than individual elements*

The Schema-PLD logic compiler runs on IBM PCs, PS/2s, and compatibles. The compiler accepts input from the vendor's schematic-capture software and compiles the design to use PLDs. When compilation is complete, the program displays the PLD resources needed so that you can then select appropriate PLDs on the basis of performance, availability, and cost. The program generates output in the form of a standard JEDEC file and comes with libraries that include most mainstream PLDs. $495.

Omation Inc, 801 Presidential Dr, Richardson, TX 75081. Phone (800) 553-9119. FAX 214-783-9072.
Circle No. 367

Op-Amp Macromodels For Spice

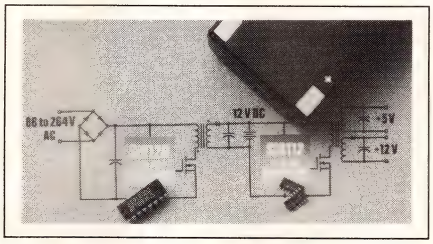
- *Disk provides new macromodels for six op amps*
- *Spice net lists included on disk*

The PMISpice library contains new, improved macromodels of the vendor's OP-42, OP-61, OP-64, OP-260, OP-400, and MAT-03 op amps. These macromodels provide much greater accuracy than the standard Boyle macromodel, especially at frequencies above 1 MHz. They are modular in structure and allow you to include any number of poles and zeros to shape the frequency response of your design. The macromodels include Spice-compatible net lists. A 2-part article scheduled for the next two issues of *EDN* will show you how to adapt these models to your own op-amp designs. PMI customers can receive the disk at no charge.

Precision Monolithics Inc, Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222. FAX 408-727-1550.
Circle No. 368

NEW PRODUCTS

INTEGRATED CIRCUITS



Switch-Mode Controllers

- *Handle high voltages*
- *Use current-mode PWM*

The Si9112 and Si9120 are current-mode PWM controllers for use in switching power supplies. Both monolithic ICs include high-voltage start-up circuitry, an oscillator, an error amplifier, a voltage reference, and a noninverted output stage for direct drive of an external power MOSFET. The Si9112 is optimized for use in dc/dc converters that operate from 12V batteries or from dc voltages in the 9 to 80V range. The Si9120 has an input-voltage capability of 50 to 450V, which makes it suitable for use in power supplies operating from 110 or 220V ac power lines. Both devices are fabricated in CMOS, which reduces the quiescent current to less than 1.5 mA. The Si9112 comes in a 14-pin DIP and in a 14-pin SOIC package; the Si9120 comes in a 16-pin DIP. $4.28 to $4.90 (100).

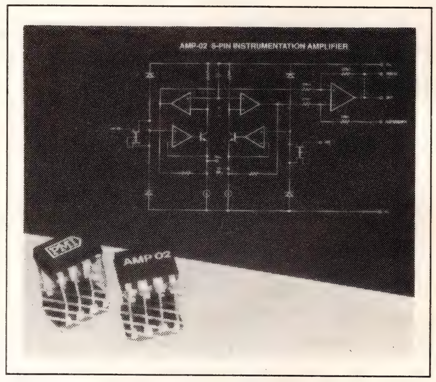
Siliconix Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 988-8000. **Circle No. 351**

16-Bit Bus Interface With Several Functions

- *Transceiver and latched multiplexer/demultiplexer*
- *Interfaces to popular backplane buses*

The SN74BCT2423 16-bit bus interface integrates four octal bus transceivers and its control circuitry in a single BiCMOS IC. Manufacturers of computers and add-in boards can use the cascadable device to interface to any popular backplane bus including the Nubus, MCA (Micro Channel Architecture) bus, and AT bus. With an available drive current of 48 mA on the multiplexed side, the interface also supports the VMEbus and Multibus. Outputs on the demultiplexed A and B buses are rated at 24 mA. The device draws only 190 mA max when enabled and 50 mA max when disabled. The SN74BCT2423, which comes in a 68-pin PLCC (plastic leaded-chip carrier), operates from a 5V supply and is characterized over the 0 to 70°C temperature range. $6.48 (1000).

Texas Instruments Inc, Box 809066, Dallas, TX 75380. Phone (800) 232-3200, ext 700.
Circle No. 352



Instrumentation Amplifier

- *Comes in an 8-pin package*
- *Features high accuracy*

The Amp-02 is a complete instrumentation amplifier in a space-saving 8-pin miniature DIP. The device, which needs only a single external resistor to set the gain, also offers internal overvoltage protection. Key specifications include an offset voltage of only 100 μV max, temperature drift of less than 2 μV/°C, a gain range of 1 to 10,000, and a minimum common-mode rejection of 115 dB. Because of its transimpedance input stage, the Amp-02 does not suffer a dramatic decrease in bandwidth as gain is increased.

At unity gain, the AMP-02 has a bandwidth of 1.2 MHz; at a gain of 1000, the bandwidth is 200 kHz. In two offset-voltage grades, $5.25 and $8.75 (100).

Precision Monolithics Inc, Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222. FAX 408-727-1550. **Circle No. 353**

10-Bit D/A Converter

- *Has 30-nsec settling time*
- *Contains on-chip data registers*

The TDC1041 is a 10-bit, 20-MHz D/A converter with a ±0.5-LSB settling time of 30 nsec. On-chip data registers eliminate the need for external registers. The outputs can directly drive 50Ω loads or complex filters, thus eliminating the need for additional amplifiers. Other features include a peak glitch area of only 25 pV/sec, differential and integral linearity errors of 0.5 LSB, and a 60-dB spurious-free dynamic range. You can operate the TTL-compatible TDC1041 without a clock signal. In a 28-pin plastic chip carrier, from $9.75 (1000).

TRW LSI Products Inc, Box 2472, La Jolla, CA 92038. Phone (619) 457-1000. FAX 619-455-6314. **Circle No. 354**

3-Chip Modem Set

- *Handles 2400 bps*
- *Complies with V.42 standards*

The SSI 73D2420 3-chip modem IC set, which can handle data rates to 2400 bps, lets designers develop products that comply with the internationally recognized V.42 LAP-M error-control standard. The set includes the 73D680 controller, 73D681 K-series interface, and 73D682 ROM. When used with one of the company's K-series single-chip modem ICs, the devices combine to provide V.42 error control, LAP-B error control, Asynchronous Framing Technique (AFT) error control, adaptive data-compression, automatic feature negotiation,

flow control, and other Hayes-compatible features. The three devices, which are available in a variety of package options, are sold as a set. $40 (10,000).

Silicon Systems, 14351 Myford Rd, Tustin, CA 92680. Phone (714) 731-7110, ext 3575.

Circle No. 355

Power Supply Control IC For Automotive Use

- *Provides current-mode PWM*
- *Has high-current totem-pole output*

Specially trimmed and tested for automotive applications, the CS-2841B provides fixed-frequency, current-mode PWM control for switch-mode power supplies. A variation of the company's CS-2843A, the CS-2841B has a typical start-threshold of 8.0V and the ability to withstand 42V automotive load-dump transients. The maximum start-threshold of 8.4V enables low-battery operation. Other features include a totem-pole output rated at ±1A max, double-pulse suppression, and pulse-by-pulse current limiting. In an 8-pin DIP, $1.09 (10,000).

Cherry Semiconductor Corp, 2000 South County Trail, East Greenwich, RI 02818. Phone (401) 885-3600. FAX 401-885-5786.

Circle No. 356

Lowpass Filters

- *Fourth- and sixth-order types*
- *Operate from 0.1 Hz to 30 kHz*

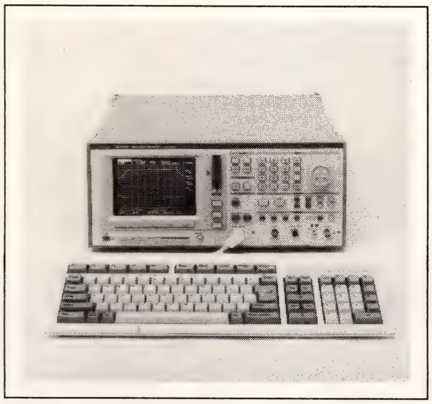
The LMF40 and LMF60 are fourth- and sixth-order lowpass filters, respectively. The filters use switched-capacitor circuitry to obtain a Butterworth response that provides an 80-dB/decade roll-off for the LMF40 and a 120-dB/decade roll-off for the LMF60. Other key specifications include a wide center-frequency range of 0.1 Hz to 30 kHz (40 kHz for the LMF40), a maximum offset voltage of 100 mV, and a typical dynamic range of 88 dB. The filters feature a clock-tunable cutoff frequency set by an internal or external clock, and a maximally flat frequency response over the passband. The devices operate from supplies of 4 to 14V or 2 to 7V. Package options include 8- and 14-pin DIPs and a 14-pin small-outline package. $2.19 to $17.20 (100), depending on temperature range and package options.

National Semiconductor Corp, Box 58090, Santa Clara, CA 95052. Phone (408) 721-2273.

Circle No. 357

NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS



1-GHz Vector Network Analyzer

- *Resolves 10^{-3} Hz from 10 kHz to 1 GHz*
- *Has a dynamic range of 120 dB*

The MS3606A vector network analyzer has a frequency resolution of 10^{-3} Hz from 10 kHz to 1 GHz and a dynamic range of 120 dB. The instrument functions as a scalar analyzer when testing devices whose inputs and outputs are at different frequencies. The instrument's frequency synthesizer switches frequencies in 150 μsec, allowing the unit to make measurements in 400 μsec. The frequency standard has an aging rate of 2×10^{-8}/day. Output is adjustable in 0.01-dB steps from −80 to +15 dBm. At 10 kHz from a 1-GHz carrier, single-sideband phase noise is 95 dB below carrier level. You can equip the unit with memory cards that store software and allow the unit to act as an instrument controller. $23,500. Delivery, 12 weeks ARO.

Anritsu America Inc, 15 Thornton Rd, Oakland, NJ 07436. Phone (800) 255-7234; in NJ, (201) 337-1111. **Circle No. 377**

Unix Instrument Drivers For PS/2 Computers

- *Work with vendor's Micro Channel IEEE-488 interface*
- *Available for SCO Xenix and IBM AIX OSs*

The NI-488M software drivers allow the vendor's MC-GPIB MCA (Micro Channel Architecture) bus IEEE-488 interface to control instruments from 80386-based IBM PS/2-family computers running under two versions of Unix. The sup-

ported operating systems are Santa Cruz Operations' SCO Xenix and IBM's AIX (Advanced Interactive Executive). The software packages include a high-speed driver, a C-language interface, and utilities for debugging application programs. The software allows porting of applications originally written to run under MS-DOS and OS/2 as well as those written for the Macintosh and for Sun workstations. NI-488M SCO Xenix, $200; NI-488M IBM AIX, $495; MC-GPIB, $495.

National Instruments, 12109 Technology Blvd, Austin, TX 78727. Phone (800) 433-3488; in TX, (512)794-0100. FAX 512-250-9319.

Circle No. 378

tute of Standards Technology, formerly the National Bureau of Standards) attests to the instrument's accuracy. $395, including a 3-year warranty.

Tegam Inc, 7230 N Ridge Rd, Madison, OH 44057. Phone (216) 428-7505. FAX 216-428-1068.

Circle No. 379

Logic Analyzer For RISC Processors

- *Supports 88000 to 50 MHz*
- *Replaces addresses with source-level-program mnemonics*

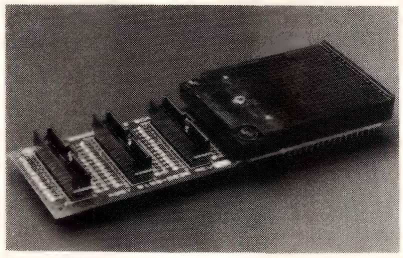
The 88000 µP-analysis package (MAP) enables the vendor's CLAS 4000 logic-analysis systems to debug systems based on Motorola's

Thermocouple Calibrator And Thermometer

- *Comes in a handheld unit*
- *J-, K-, and T-type compatible*

The model 840 is a handheld, combined calibrator and digital-readout thermometer suitable for use with J-, K-, and T-type thermocouples. You can generate or measure thermocouple voltage levels with a full-range resolution of 0.1°F over a range of −340 to +2500°F. In both calibrate and measure modes, you can store 10 points in nonvolatile memory. A calibration certificate traceable to NIST (National Insti-

88000 series RISC processors. The analyzer supports chips operating at 50 MHz—the fastest clock speed Motorola currently offers. The package includes a 1.75-in.-square, low-profile socket for the μP and a disassembler that lets you replace addresses with mnemonics from the source-level program. The disassembly display shows all bus cycles with type information and mnemonics and lets you delete unexecuted instructions and data read/write cycles. The unit loads the μP signals minimally (1 MΩ in parallel with 10 pF), resolves event timing to 5-nsec, and captures 3-nsec glitches. $2950; CLAS 4000, from $19,950.



Gould Inc, 19050 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 538-9320. FAX 408-988-1647.
Circle No. 380

60- And 100-MHz Bandwidth DSOs

- *Acquire 250M samples/sec*
- *Reproduce transients containing 25-MHz information*

The PM 3355 and PM 3375 DSOs (digital storage oscilloscopes) acquire 250M samples/sec. With repetitive signals, the PM 3355 has an analog bandwidth of 60 MHz; the corresponding figure for the PM 3375 is 100 MHz. When you use the scopes to capture single-shot phenomena, the vendor recommends that you take 10 samples/cycle of the highest frequency component of interest. Hence you can use the scopes to capture transients that contain 25-MHz information. Vertical resolution is 8 bits, and signal averaging improves the S/N ratio of repetitive signals. Both scopes have four acquisition memories each of which holds 4k samples. Both units trigger on 150-MHz signals and provide post triggering to 5000 divisions. LCD panels adjacent to the screen indicate control settings. PM 3355, $4500; PM 3375, $5390.

John Fluke Mfg Co Inc, Box C9090, Everett, WA 98206. Phone (800) 443-5853, ext 77. TLX 185102.
Circle No. 381

Philips Test and Measurement, Bldg HKF, 5600 MD, Eindhoven, The Netherlands. Phone local office. **Circle No. 382**

EDN
PRODUCT MART

This advertising is for new and current products.

Please circle Reader Service number for additional information from manufacturers.

X.25 SDLC
QLLC HDLC
ADCCP PAD

- C source code
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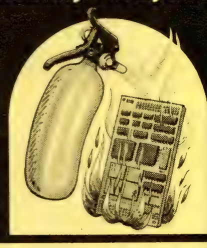

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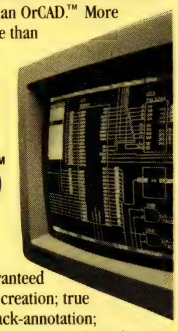

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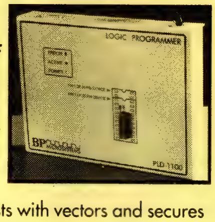

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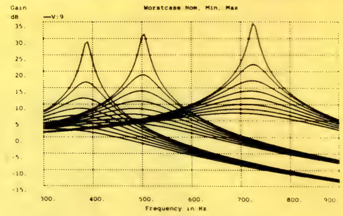

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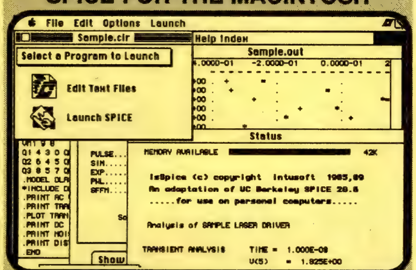

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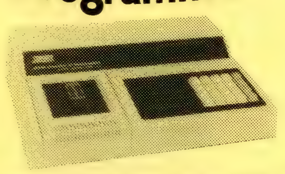

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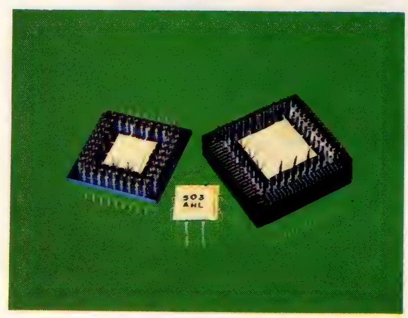

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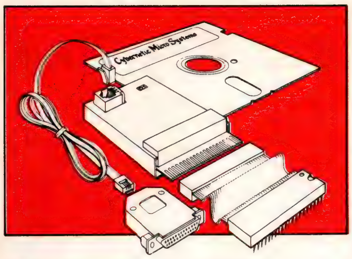

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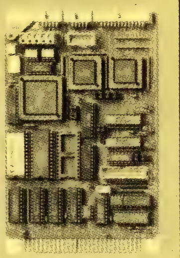

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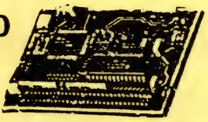

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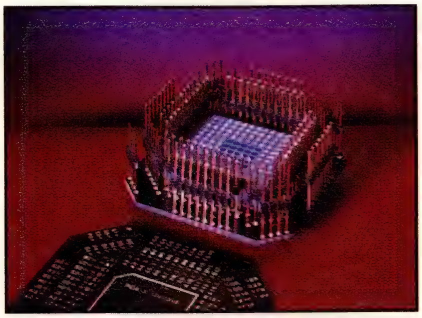

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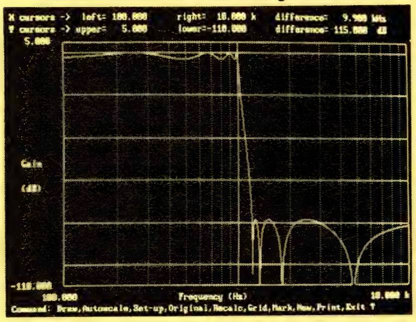

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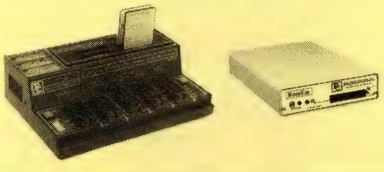

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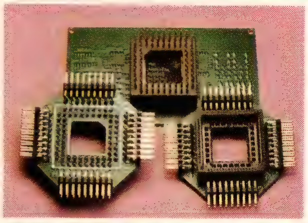

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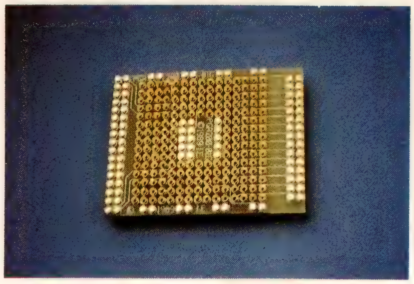

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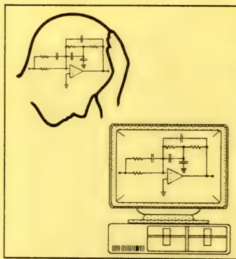

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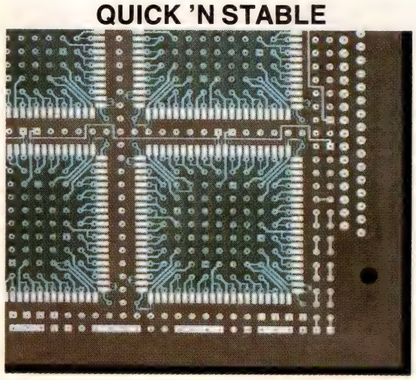

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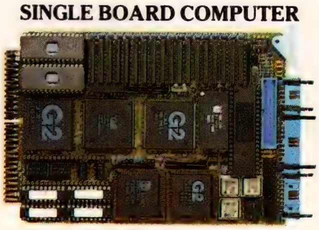

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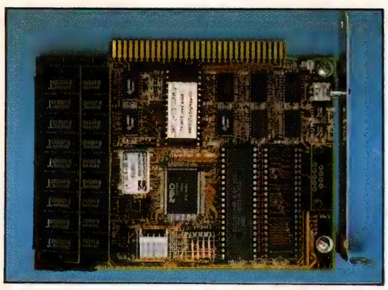

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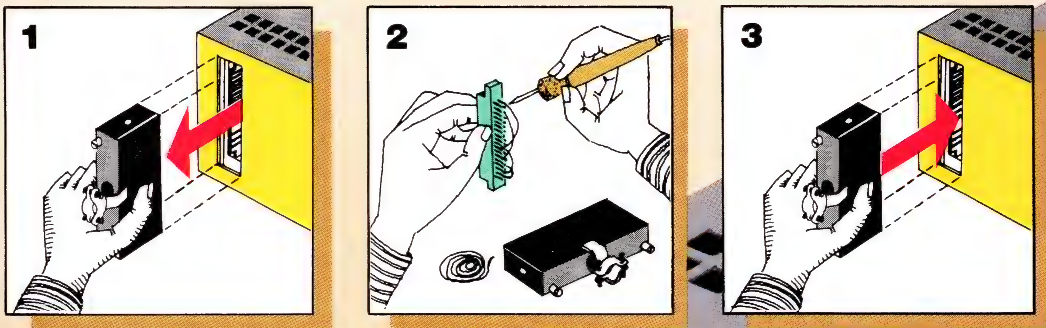
Your Kepco ATE Power Manager, like most *conventional* power supplies, is delivered with large output and feedback capacitors connected. This equips it to give you a rock steady voltage in the face of varying load currents.

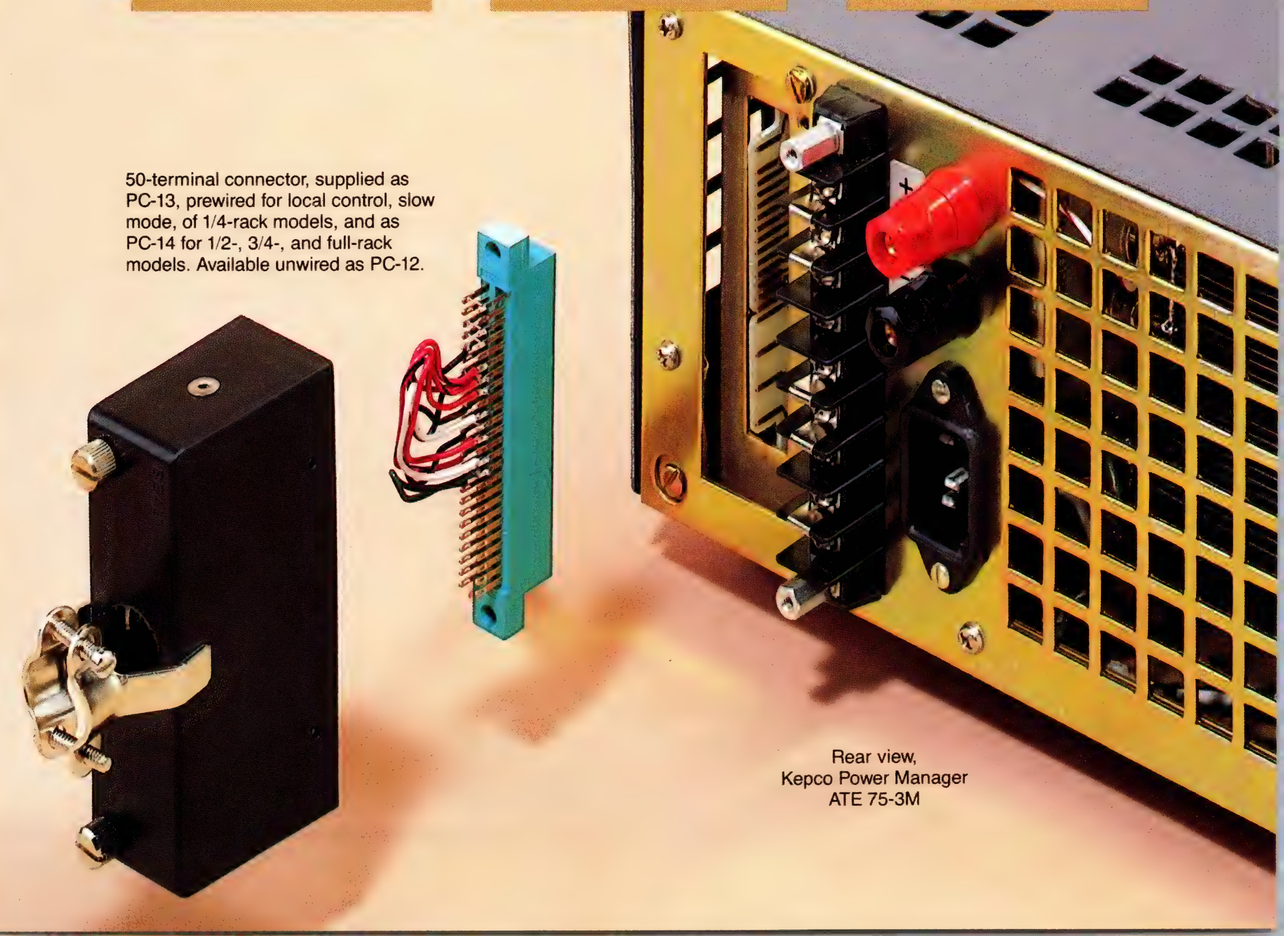
The ATE, however, is no conventional power supply. The thing that makes it *un*conventional is the 50-terminal user port at the rear.

By simply **(1)** pulling out the mating connector, **(2)** rewiring it, and **(3)** putting it back, you can *in a matter of minutes* obtain access to a host of control functions. You can, for example, cut out the output and feedback capacitors and configure your ATE* to give you a steady *current* against a varying *voltage*. Better yet, buy a blank connector (they're only $18 apiece) and wire it up in the current stabilizer configuration. Then, you can make the transformation in moments.

What the Kepco user port does is give you the ability to connect any element in the ATE's control assembly with nearly any other. So the way you wire it determines the nature of the ATE. One configuration lets you control the voltage channel with a 0-10V analog d-c signal (or a digital signal via a Kepco SN or TLD digital interface); another lets you control the current channel with a 0-1V signal. Other configurations let you control voltage or current with a 2-terminal resistance, or a high impedance source; others turn your ATE into a self-powered, oversized op amp or a servo amplifier. And still others let you use the uncommitted amplifiers we've included in the ATE's control assembly, to sum, scale, invert, or integrate control signals. The possibilities are limited only by your imagination.

*On Size E models, you must also remove a link from the rear barrier strip.





50-terminal connector, supplied as PC-13, prewired for local control, slow mode, of 1/4-rack models, and as PC-14 for 1/2-, 3/4-, and full-rack models. Available unwired as PC-12.

Rear view,
Kepco Power Manager
ATE 75-3M

STATIC STABILIZATION TABLE

INFLUENCE QUANTITY	OUTPUT EFFECTS VOLTAGE MODE Typ.	Max.	OUTPUT EFFECTS CURRENT MODE Typ.	Max.	OFFSETS [4] ΔE_{io}	ΔI_{io}
SOURCE VOLTAGE (min.–max.):	<0.0005% E_0 max.	0.001% E_0 max.	<0.002% I_0 max.	0.005% I_0 max.	<1 µV	<1 nA
LOAD (no load–full load):	<0.001% E_0 max.	0.002% E_0 max.	<0.5 mA[1]	1 mA[1]	—	—
TIME (8-hour drift):	<0.005% E_0 max.	0.01% E_0 max.	<0.01% I_0 max.	0.02% I_0 max.	<20 µV	<1 nA
TEMPERATURE, per °C:	<0.005% E_0 max.	0.01% E_0 max.	<0.01% I_0 max.	0.02% I_0 max.	<20 µV	<2 nA
RIPPLE and NOISE[2] rms:	<0.1 mV	0.3 mV	<0.01% I_0 max.	0.03% I_0 max.	—	—
(Slow Mode) p-p:[3]	<1 mV	3 mV	<0.1% I_0 max.	0.3% I_0 max.	—	—
RIPPLE and NOISE[2] rms:	<1 mV	3 mV	<0.01% I_0 max.	0.03% I_0 max.	—	—
(Fast Mode) p-p:[3]	<10 mV	30 mV	<0.1% I_0 max.	0.3% I_0 max.	—	—

(1) For models with output current rating of 50A and higher, the load effect is 2 mA typical and 5 mA maximum. In slow mode, the leakage current through the output capacitor adds approximately 0-6 mA to the current mode load effect.
(2) One terminal must be grounded for this measurement, or connected so that common mode current does not flow through the load or, in current mode, through the current-sensing resistor.
(3) Peak-to-peak ripple is measured over a 20 Hz to 10 MHz bandwidth.
(4) Uncommitted amplifier offsets.

GENERAL

Crowbar trigger time:
Slow mode — 50µsec.
Fast mode — 500µsec delay, to avoid false triggering.

OVP action:
1) Short output with SCR.
2) Trip a-c circuit breaker.
3) Generate optically isolated flag signal.

Series operation:
To the 500V limit of the isolation voltage; master/slave operation is possible.

Parallel operation:
Master/slave operation, and redundant connections, are possible.

Isolation:
Output may be floated up to 500V off ground. Common mode current — 5µA rms, 50µA peak to peak, at 115V a-c.

Temperature:
Storage — −40°C to 85°C.
Operating — 0°C to +55°C (derate to 90% of rated current at +65°C.)

Cooling:
Built-in fan (2 in full-rack models) exhausts air to rear.

D-C output terminal (Rear):
1/4-rack models — barrier strip.
1/2- and 3/4-rack models — binding posts.
Full-rack models — compression studs.

Meters:
1/4- and 1/2-rack models: Two 1½", 3%
3/4- and full-rack models: Two 2½", 2%

Source voltage:
User selectable, 95-113, 105-125, 190-226, or 210-250V a-c, 50-65 Hz, single phase; do not use on 400Hz.

Source current:
See Table 1.

Output current:
Continuously adjustable or programmable, 0-100%.

Control voltage:
Local — 10-turn rheostat on front panel.
Remote — 0 to 10V signal.

Control current:
Local — 10-turn rheostat on front panel.
Remote — 0 to 1V signal.

Remote error sensing:
Provision made for 4-terminal connection to load; static drop of 0.5V/lead may be compensated, and an extra volt is provided for this purpose.

Program speed (programming time constant, [τ]):
Slow mode — $[\tau] = R_1 \times C_{out}$ (see model tables).
Fast mode — see Table 2.

Current recovery for a step load voltage:
Exponential with programming time constant, [τ].

Mode Indicators
Voltage — green LED, front panel.
Current — amber LED, front panel.
OVP — red LED, front panel.

Mode flags
TTL logic signals delivered to rear connector as optically isolated outputs.

OVP control:
Local — trimmer adjustable.
Remote — 0-10V signal, or may be set to track output voltage.

Remote trigger:
Optically isolated "trigger-in" port allows overvoltage tripping by remotely generated pulse, so that OVPs of several power supplies can be interconnected or sequenced or simultaneous shutdown. Lower limit for OVP is 3V, adjustable to 110% E_0. Minimum threshold adjustment: 0.5V or 2%E_0, whichever is greater.

Table 1 Source Current

(Measured, worst case, at 125V a-c source voltage)
Size A-1.4A max.
Size B-2.4A max.
Size C-6.0A max.
Size D-11.0A max.
Size E-20.0A max.

Table 2 Dynamic Specifications

Output Voltage Ratings	Bandwidth (−3dB) KHz Min.	Programming Time Constant (µsec) Max.
6V	16.0	10.0
15V	10.6	15.0
25V	8.0	20.0
36V	6.4	25.0
55V	4.0	40.0
75V	3.5	45.0
100V	2.5	65.0
150V	1.7	95.0
325V	0.94	170.0

Voltage recovery: For step load change between 10% and 100% I_0 maximum <50 µsec typ., <100 µsec max. to recover within 10mV

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ATE MODELS • QUARTER • HALF • THREE-QUARTER • FULL RACK

ACCESSORY FOR RACK MOUNTING: RA 37

50 WATTS
0-55°C No Derating
QUARTER RACK SIZE A

MODEL	D-C OUTPUT RANGE		OUTPUT IMPEDANCE VOLTAGE MODE			OUTPUT IMPEDANCE CURRENT MODE		
	VOLTS	AMPS	SERIES RESISTANCE	SERIES INDUCTANCE SLOW	FAST	SHUNT(2) RESISTANCE	SHUNT CAPACITANCE SLOW	FAST
ATE 6-5M	0-6	0-5	24 µΩ	0.5 µH	5 µH	12 kΩ	1,000 µF	1 µF
ATE 15-3M	0-15	0-3	100 µΩ	0.5 µH	5 µH	30 kΩ	450 µF	0.4 µF
ATE 25-2M	0-25	0-2	250 µΩ	1 µH	10 µH	50 kΩ	250 µF	0.25 µF
ATE 36-1.5M	0-36	0-1.5	480 µΩ	1 µH	10 µH	72 kΩ	200 µF	0.2 µF
ATE 55-1M	0-55	0-1	1.1 mΩ	2 µH	20 µH	110 kΩ	150 µF	0.15 µF
ATE 75-0.7M	0-75	0-0.7	2.15 mΩ	2 µH	20 µH	150 kΩ	110 µF	0.1 µF
ATE 100-0.5M	0-100	0-0.5	4 mΩ	4 µH	40 µH	200 kΩ	50 µF	0.05 µF
ATE 150-0.3M	0-150	0-0.3	10 mΩ	4 µH	40 µH	300 kΩ	55 µF	0.02 µF

Size: 5 7/32″ H x 4 5/32″ W x 17 1/8″ D (132.6mm H x 105.6mm W x 435.0mm D)(1) **Net Weight:** 14 lbs. (6.4 kg.)

100 WATTS
0-55°C No Derating
QUARTER RACK SIZE B

MODEL	D-C OUTPUT RANGE		OUTPUT IMPEDANCE VOLTAGE MODE			OUTPUT IMPEDANCE CURRENT MODE		
	VOLTS	AMPS	SERIES RESISTANCE	SERIES INDUCTANCE SLOW	FAST	SHUNT(2) RESISTANCE	SHUNT CAPACITANCE SLOW	FAST
ATE 6-10M	0-6	0-10	12 µΩ	0.5 µH	5 µH	12 kΩ	1,800 µF	2 µF
ATE 15-6M	0-15	0-6	50 µΩ	0.5 µH	5 µH	30 kΩ	1000 µF	0.8 µF
ATE 25-4M	0-25	0-4	125 µΩ	1 µH	10 µH	50 kΩ	500 µF	0.5 µF
ATE 36-3M	0-36	0-3	240 µΩ	1 µH	10 µH	72 kΩ	350 µF	0.4 µF
ATE 55-2M	0-55	0-2	0.55 mΩ	2 µH	20 µH	110 kΩ	200 µF	0.3 µF
ATE 75-1.5M	0-75	0-1.5	1 mΩ	2 µH	20 µH	150 kΩ	110 µF	0.2 µF
ATE 100-1M	0-100	0-1	2 mΩ	4 µH	40 µH	200 kΩ	80 µF	0.1 µF
ATE 150-0.7M	0-150	0-0.7	4 mΩ	4 µH	40 µH	300 kΩ	55 µF	0.04 µF

Size: 5 7/32″ H x 4 5/32″ W x 17 1/8″ D (132.6mm H x 105.6mm W x 435.0mm D)(1) **Net Weight:** 17 lbs. (7.7 kg.)

ACCESSORY FOR RACK MOUNTING: RA 37

250 WATTS
0-55°C No Derating
HALF RACK SIZE C

MODEL	D-C OUTPUT RANGE		OUTPUT IMPEDANCE VOLTAGE MODE			OUTPUT IMPEDANCE CURRENT MODE		
	VOLTS	AMPS	SERIES RESISTANCE	SERIES INDUCTANCE SLOW	FAST	SHUNT(2) RESISTANCE	SHUNT CAPACITANCE SLOW	FAST
ATE 6-25M	0-6	0-25	4.8 µΩ	0.5 µH	5 µH	12 kΩ	11,000 µF	5 µF
ATE 15-15M	0-15	0-15	20 µΩ	0.5 µH	5 µH	30 kΩ	5,800 µF	2 µF
ATE 25-10M	0-25	0-10	50 µΩ	1 µH	10 µH	50 kΩ	2,900 µF	1.25 µF
ATE 36-8M	0-36	0-8	90 µΩ	1 µH	10 µH	72 kΩ	2,400 µF	1 µF
ATE 55-5M	0-55	0-5	0.22 mΩ	2 µH	20 µH	110 kΩ	1,400 µF	0.75 µF
ATE 75-3M	0-75	0-3	0.5 mΩ	2 µH	20 µH	150 kΩ	850 µF	0.5 µF
ATE 100-2.5M	0-100	0-2.5	0.8 mΩ	4 µH	40 µH	200 kΩ	375 µF	0.25 µF
ATE 150-1.5M	0-150	0-1.5	2 mΩ	4 µH	40 µH	300 kΩ	275 µF	0.1 µF
ATE 325-0.8M	0-325	0-0.8	8.1 mΩ	100 µH	1 mH	650 kΩ	180 µF	0.01 µF

Size: 5 7/32″ H x 8 11/32″ W x 17 9/64″ D (132.6mm H x 211.9mm W x 435.4mm D)(1) **Net Weight:** 35 lbs. (15.9 kg.)

ACCESSORY FOR RACK MOUNTING: RA 37

500 WATTS
0-55°C No Derating
THREE-QUARTER RACK SIZE D

MODEL	D-C OUTPUT RANGE		OUTPUT IMPEDANCE VOLTAGE MODE			OUTPUT IMPEDANCE CURRENT MODE		
	VOLTS	AMPS	SERIES RESISTANCE	SERIES INDUCTANCE SLOW	FAST	SHUNT(2) RESISTANCE	SHUNT CAPACITANCE SLOW	FAST
ATE 6-50M	0-6	0-50	2.4 µΩ	0.5 µH	5 µH	12 kΩ	12,000 µF	10 µF
ATE 15-25M	0-15	0-25	12 µΩ	0.5 µH	5 µH	30 kΩ	8,000 µF	4 µF
ATE 25-20M	0-25	0-20	25 µΩ	1 µH	10 µH	50 kΩ	5,800 µF	2.5 µF
ATE 36-15M	0-36	0-15	48 µΩ	1 µH	10 µH	72 kΩ	4,900 µF	2 µF
ATE 55-10M	0-55	0-10	0.11 mΩ	2 µH	20 µH	110 kΩ	2,900 µF	1.5 µF
ATE 75-8M	0-75	0-8	0.19 mΩ	2 µH	20 µH	150 kΩ	1,200 µF	1 µF
ATE 100-5M	0-100	0-5	0.4 mΩ	4 µH	40 µH	200 kΩ	600 µF	0.5 µF
ATE 150-3.5M	0-150	0-3.5	0.86 mΩ	4 µH	40 µH	300 kΩ	440 µF	0.2 µF

Size: 5 7/32″ H x 12 17/32″ W x 17 9/64″ D (132.6mm H x 318.3mm W x 435.4mm D)(1) **Net Weight:** 43 lbs. (19.5 kg.)

The full rack model is supplied with brackets for direct mounting in a standard 19-inch rack.

1000 WATTS
0-55°C No Derating
FULL RACK SIZE E

MODEL	D-C OUTPUT RANGE		OUTPUT IMPEDANCE VOLTAGE MODE			OUTPUT IMPEDANCE CURRENT MODE		
	VOLTS	AMPS	SERIES RESISTANCE	SERIES INDUCTANCE SLOW	FAST	SHUNT(2) RESISTANCE	SHUNT CAPACITANCE SLOW	FAST
ATE 6-100M	0-6	0-100	1.2 µΩ	0.5 µH	5 µH	12 kΩ	22,000 µF	15 µF
ATE 15-50M	0-15	0-50	6 µΩ	0.5 µH	5 µH	30 kΩ	12,000 µF	6 µF
ATE 25-40M	0-25	0-40	12.5 µΩ	1 µH	10 µH	50 kΩ	11,000 µF	4 µF
ATE 36-30M	0-36	0-30	24 µΩ	1 µH	10 µH	72 kΩ	9,500 µF	3 µF
ATE 55-20M	0-55	0-20	55 µΩ	2 µH	20 µH	110 kΩ	5,200 µF	2.25 µF
ATE 75-15M	0-75	0-15	0.1 mΩ	2 µH	20 µH	150 kΩ	3,400 µF	1.5 µF
ATE 100-10M	0-100	0-10	0.2 mΩ	4 µH	40 µH	200 kΩ	1,200 µF	0.75 µF
ATE 150-7M	0-150	0-7	0.42 mΩ	4 µH	40 µH	300 kΩ	1,050 µF	0.3 µF

Size: 6 31/32″ H x 16 1/2″ W x 20 1/64″ D (177.0mm H x 419.1mm W x 508.4mm D)(1) **Net Weight:** 87 lbs. (39.5 kg.)

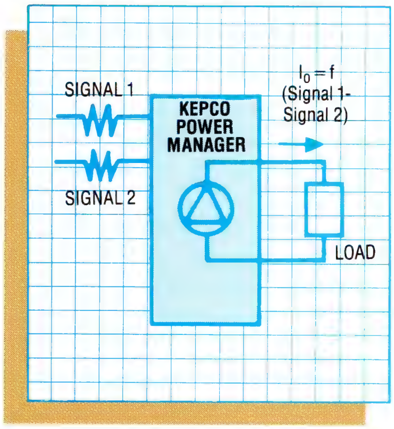
(1)Add 2 1/2″ (63.5mm) for connector protrusion. (2)Based on 0.5 mA load effect in FAST mode.
(3)For determining dynamic impedance in voltage mode. (4) For determining dynamic impedance in current mode.

Kepco ATE Power Managers are unipolar linear programmable power supplies that give you full external control over both voltage and current, with automatic crossover. They have panel-mounted meters for monitoring both channels, and front panel LEDs (and optically isolated flags accessible through the user port) to tell you which channel is in charge. Local control is by panel-mounted 10-turn rheostats.

TEAR ON DOTTED LINE TO REMOVE AND SAVE.

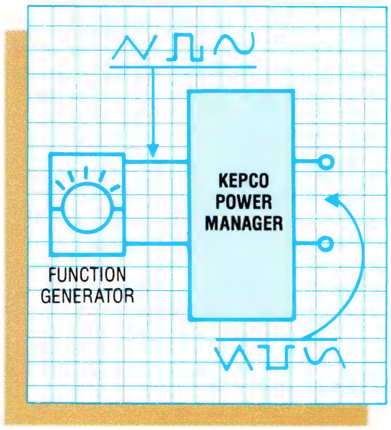
ATE POWER SUPPLIES
50 Watts to 1000 Watts

ATE CAN SUM INPUT CONTROL SIGNALS



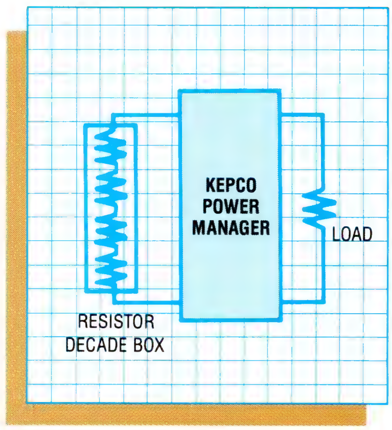
A current stabilizer controlled by the difference between two signals

...BE DRIVEN BY AN ANALOG FUNCTION



A voltage stabilizer controlled by a signal generator

OR INTERFACE TO THE DIGITAL WORLD (See back cover).



A voltage stabilizer controlled by a passive resistance decade box

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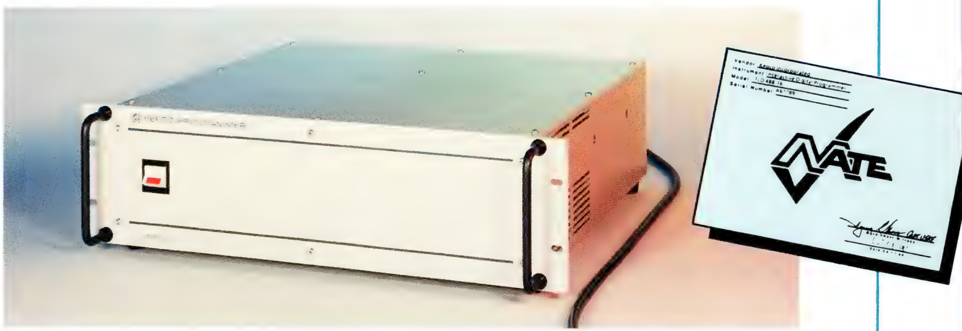
Kepco's Series ATE power supplies are "MATE-verified" for use in Modular Automatic Test Equipment that is addressed in the (CIIL) Control Interface Intermediate Language.

Kepco's TLD 488-16 interactive digital interface is an IEEE-488-driven talker-listener that has been verified as a TMA (Test Module Adapter) for Kepco's ATE and BOP(1) power supplies.



On October 1, 1987 Kepco's TLD officially achieved "MATE-verified" status.
The certificate shown was issued by the MATE program office, Kelly AFB, Texas.

The TLD 488-16 responds to commands in CIIL (Control Interface Intermediate Language) over the IEEE-488 bus from your computer or digital controller, and passes them along to the Power Managers under its control. It can control up to 16 Kepco ATE and/or BOP Power Managers at once, and if one of them cannot obey a command, it sends back a flag which the TLD 488-16 translates into CIIL and passes along to the controller as an "error message." Among the error messages it can send are "crowbarred," "overload," "voltage comparison error," and "current comparison error."

You can give your commands to the TLD 488-16 directly in Volts and Amps, because it knows the voltage and current ranges of every Power Manager under its control and can calculate what percentage of full scale a given voltage or current setting is.

(1) BOP are Kepco Bipolar Power Supplies. Please see brochure 146-1636.

Kepco Series ATE power supplies may be listener-addressed using a selection of 1-, 4- and 8-channel digital interfaces.

SN 488 works with the IEEE-488 bus, and SN 500 works with buses using bit-parallel data transfer, but they're otherwise identical. They're both available with one channel or with two isolated channels, and if you buy a single channel model, you can buy a field-installable second channel any time you need it.

SNR 488-4 and SNR 488-8 are card cages into which you can plug four to eight dual channel programming cards.

Output of all SN cards is 0 to ±1V or 0 to ±10V selectable, and all offer models that accept data in 12-bit hex or 3 digit BCD.

TYPE SN STAND ALONE INTERFACE

	SINGLE AND DUAL CHANNEL PROGRAMMERS, 1/4-RACK SIZE							
	SN488-				SN500-			
MODEL	121	122	031	032	121	122	031	032
NUMBER OF CHANNELS	1	2	1	2	1	2	1	2
INPUT DATA CODING FORMAT	Hex		Decimal		Hex		Decimal	
RESOLUTION	12 Bit		3 Digit		12 Bit		3 Digit	

TYPE SNR 488-4
(Addresses up to 4 ATE power supplies)

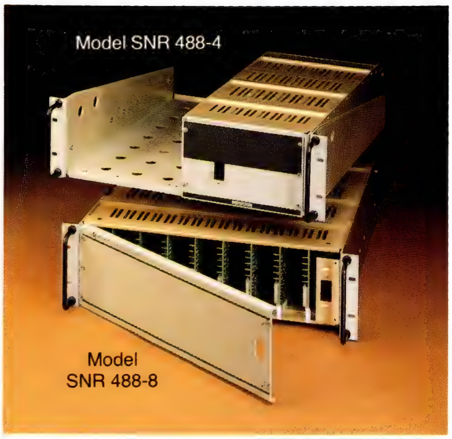
TYPE SNR 488-8
(Addresses up to 8 ATE power supplies)

SNR Housings

MODEL	HOLDS
SNR 488-4	4 Cards
SNR 488-8	8 Cards

Interface cards

MODEL	DATA FORMAT	RESOLUTION
SN 488-B	Hex	12-bit binary
SN 488-D	Decimal	3-digit BCD



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CAREER OPPORTUNITIES

1990 Recruitment Editorial Calendar

Issue	Issue Date	Ad Deadline	Editorial Emphasis
Magazine Edition	Mar. 1	Feb. 8	Computer-Aided Engineering/ASICs, Computers & Peripherals, Digital ICs/Microprocessors, Semicustom ICs
News Edition	Mar. 8	Feb. 15	Analog/ICs, Automotive Electronics, Special Supplement: RISC/Microprocessors
Magazine Edition	Mar. 15	Feb. 22	Analog ICs, Components, Engineering Software, Special Design Project #1
News Edition	Mar. 22	Mar. 2	Optoelectronics, Peripherals, Regional Profile: New York, Pennsylvania & Connecticut
Magazine Edition	Mar. 29	Mar. 8	Software Special Issue—Interface ICs, Software/Programming/Microprocessors/ASICs, April Fools Section, Special Design Project #2
News Edition	Apr. 5	Mar. 16	IC/Logic ICs, Distribution, Special Supplement: Distribution
Magazine Edition	Apr. 12	Mar. 22	Communications Special Issue—Communication ICs, Communication Systems, Microprocessors, Special Design Project #3
News Edition	Apr. 19	Mar. 30	ICs/Graphics Controllers/Microprocessors, Industrial Automation, Regional Profile: So. California
Magazine Edition	Apr. 26	Apr. 5	Computer Boards/Microprocessors, Power Sources, Sensors/Transducers, Special Design Project #4, Electro Show Issue
News Edition	May 3	Apr. 12	CAE/Board Layout, Education, Special Supplement: ASICs, Electro Show Issue
Magazine Edition	May 10	Apr. 19	Analogy Technology Special Issue—Analog ICs, Analog Instruments, Digital ICs/Microprocessors/ASICs, Special Design Project #5
News Edition	May 17	Apr. 27	ICs/Memory ICs, Test & Measurement, Regional Profile: Massachusetts & New Hampshire
Magazine Edition	May 24	May 3	Microprocessors, Computers & Peripherals, Semicustom ICs/ASICs, Components, Sensors & Transducers
Magazine Edition	June 7	May 17	Software, Design Tools, Microprocessor I/O Chips, μP Support Chip Directory
News Edition	June 14	May 24	Peripherals/Input Devices, Software, Special Supplement: EDA
Magazine Edition	June 21	May 31	Computer-Aided Engineering, Computers & Peripherals, Power Semiconductors, Semicustom ICs/ASICs
News Edition	June 28	June 8	ICs/RISC/Microprocessors, Image Processing, Regional Profile: Oregon & Washington
Magazine Edition	July 5	June 14	Product Showcase—Volume I: Hardware & Interconnect, Power Sources, ICs & Semiconductors, Software
News Edition	July 12	June 21	Analog/Communication ICs, ASICs, Special Supplement: Automotive Electronics, Regional Profile: Washington, D.C.
Magazine Edition	July 19	June 28	Product Showcase—Volume II: CAE/ASICs, Computers & Peripherals, Components, Test & Measurement
Magazine Edition	Aug. 2	July 12	Digital ICs/Microprocessors, Computer-Aided Engineering, Computers & Peripherals, Test & Measurement, Technical Article Database
News Edition	Aug. 9	July 20	CAE/Software, Aerospace, Special Supplement: Defense
Magazine Edition	Aug. 20	July 30	Military Special Issue, Vision/Image Systems, ICs & Semiconductors, Memory Technology, Software
News Edition	Aug. 23	Aug. 3	Electromechanical, Opportunities in Non-EOEM, Regional Profile: New Mexico, Arizona
Magazine Edition	Sept. 3	Aug. 13	ASICs Special Issue—Semicustom ICs, Computer-Aided Engineering, Digital Components, ICs & Semiconductors
News Edition	Sept. 6	Aug. 17	CAE/Software, CASE/CAE, Special Supplement: DSP

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Lead the electrical design of motion control, data acquisition and high-voltage subsystems from concept through manufacturing.

UNIX SOFTWARE PROJECT LEADER:

Sun, Unix languages, computer-aided development tools.

REAL-TIME SOFTWARE ARCHITECT:

C, Unix, Sun, process control, communications.

LOW LEVEL ANALOG DATA ACQUISITION:

Custom sub pico-amp, 20 bit data acquisition systems, low noise circuit design, hi-speed, multi-channel data acquisition.

DIGITAL SIGNAL PROCESSING:

Algorithm to circuitry translation, DSP, ASIC, hi-speed signal distribution, Mentor circuit stimulation, use of design tools for gate array and Xilinx design/simulation.

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Develop mechanical structure and packaging design using Apollo CAD tools.

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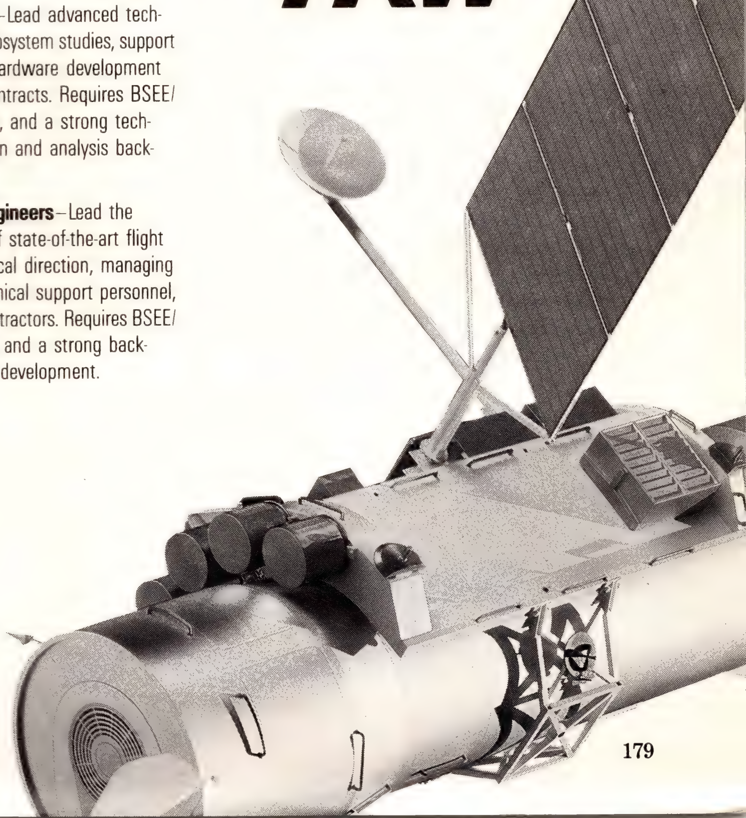

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- **Digital Design**
- **Test/Diagnostic Software**
- **Microwave Oscillator Source & Receiver Design**
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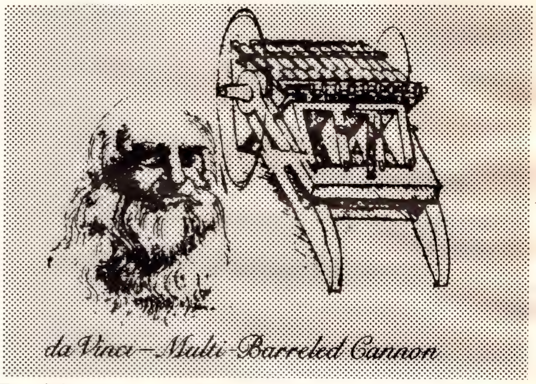

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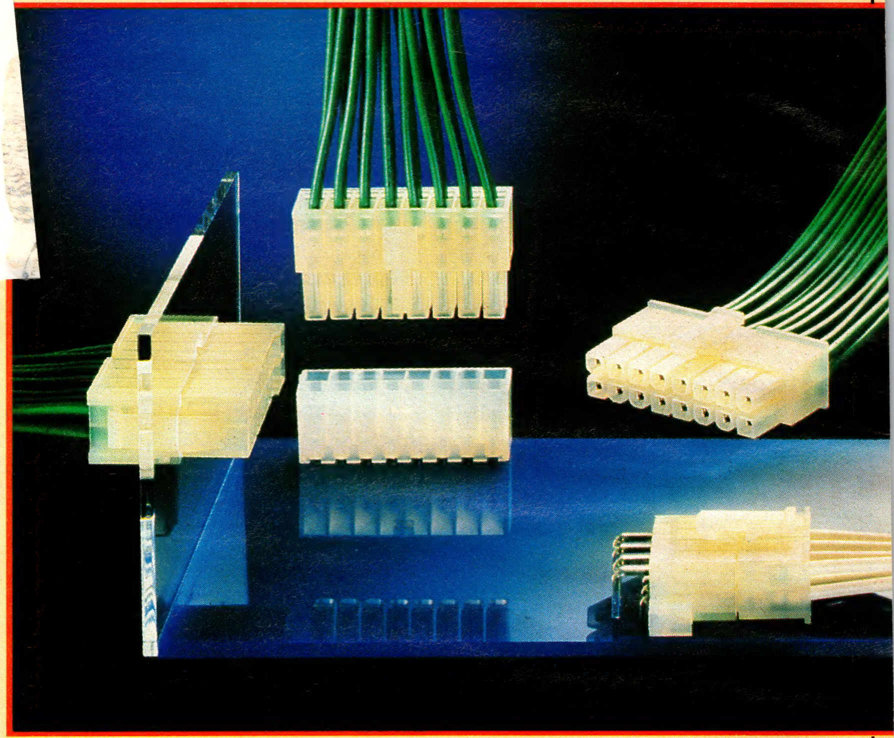

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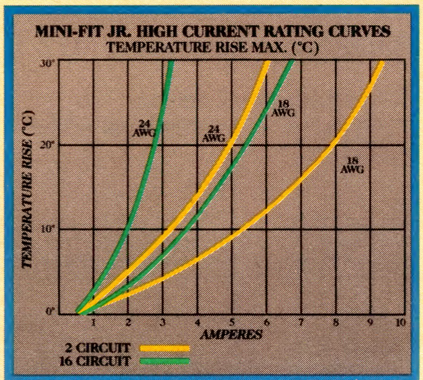

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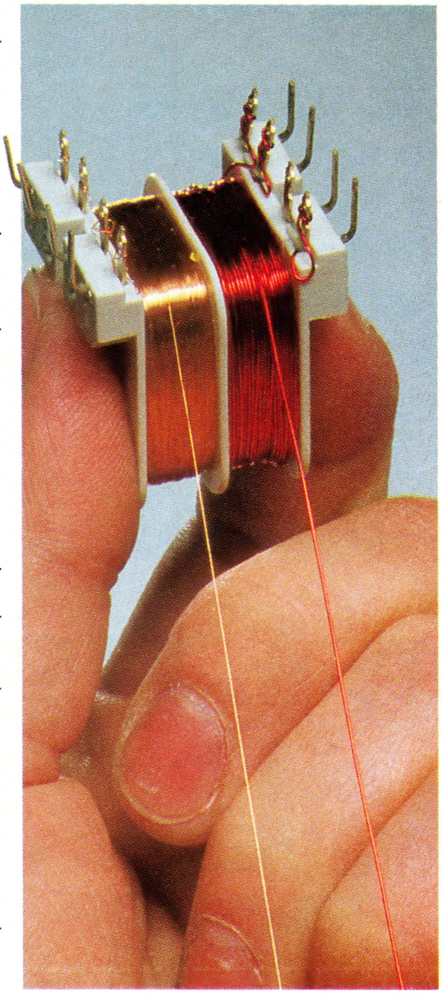

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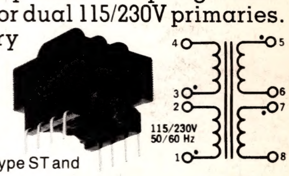

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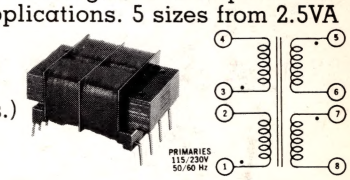

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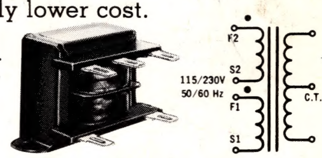

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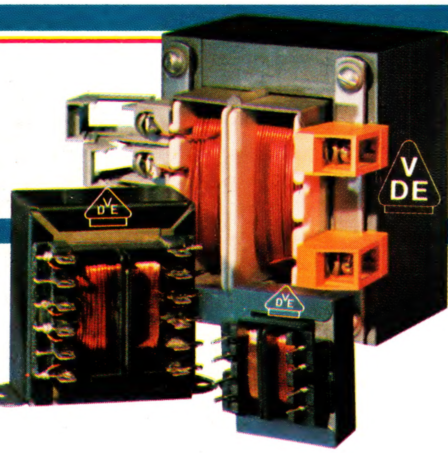

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